

High Performance Configurable Digital AC Servo Control IC

Features

- **Complete closed loop current control (Synchronously Rotating Frame Field Orientation)**
- **Versatile Space Vector PWM**
- **Direct interface to IR2175 current sensing high voltage IC**
- **Direct Encoder interface with multiplexed/non-multiplexed Hall A/B/C signals**
- **Direct interface to IR213x 3-phase gate driver IC**
- **Closed loop velocity control**
- **Configurable architecture**
 - **Supports AC PM motor or Induction motor**
 - **Closed loop or open loop control**
- **Asynchronous serial communication interface (RS232C, RS422)**
- **Fast SPI interface**
- **4 channel 12-bit A/D interface with simultaneous sample/hold**
- **8-bit parallel bus interface for microcontroller expansion (supports most 8-bit microprocessors)**
- **Integrated brake IGBT control**
- **ServoDesigner™ (Configuration Tool) available**

Product Summary

| | |
|--|--------------|
| Max. Clock Input (Sysclk) | 33.3 MHz |
| Max. PLL clock for current feedback | 133.3 MHz |
| Closed loop current control computation time | 6 µsec max |
| Closed loop current loop bandwidth (-3 dB) | 5.5 kHz |
| Closed loop velocity loop update rate | 5 / 10 kHz |
| PWM carrier frequency | 83.3 kHz max |
| PWM counter resolution | 12 bit |
| Current feedback temp drift/offset | calibrated |
| Max SPI clock | 8 MHz |
| Package: | QFP100 |



Description

IRMCK201 is a complete AC servo motor control IC. It contains closed loop current control for sinusoidal AC current, and closed loop velocity control based on encoder position feedback interface. A standard communication port is provided for RS232C or RS422, in addition to a fast SPI communication interface. Unlike a traditional DSP or a microcontroller, the IRMCK201 does not require any programming effort to complete the complex control algorithm. It allows users to configure the algorithm for specific application needs. Permanent magnet motor or AC induction motor are supported. IRMCK201 facilitates high performance servo design together with the IR2175 current sensing IC and IR213x high voltage 3-phase gate driver IC, which simplifies the hardware design while minimizing cost. For multi-axis applications, IRMCK201 can be used as a multi-drop slave drive based on the SPI protocol. The package is available in a 100-pin QFP.

Overview

IRMCK201 is a new International Rectifier integrated circuit device designed as a one-chip solution for complete closed loop current control and velocity control for a high performance servo drive system. Unlike a traditional microcontroller or DSP, IRMCK201 does not require any programming to complete complex AC servo algorithm development. Combined with International Rectifier's high voltage gate drive and current sensing IC, the user can implement a complete AC servo control with minimum component count and virtually no design effort. Although IRMCK201 contains dedicated logic to perform closed loop control of AC current and velocity, it has a wide range of application coverage through its flexible configuration ability. The drive can be easily configured for induction machine closed loop vector control or permanent magnet motor servo drive. Rich motion peripherals, analog and digital I/O can also be configured. Host communication logic contains an asynchronous RS232C or RS422 communication interface, a fast slave SPI interface and an 8-bit-wide Host Parallel Interface. All communication ports have the same access capability to the host register set. The user can write to and read from the predefined registers to configure and monitor the drive through these communication ports.

IRMCK201 Main Features

IRMCK201 contains the following functions for AC servo motor control applications:

- Complete closed loop current control based on Synchronously Rotating Frame Field Orientation
- Configurable update rate with PWM carrier frequency
- Configurable parameters (all PI controller gains, PI output limit range, current feedback scaling, encoder feedback scaling)
- Configurable control structure for Induction machine or AC Permanent Magnet machine (Disable/enable slip gain)
- Closed loop velocity control with configurable update rate
- Enable/disable velocity loop
- Selectable reference input for torque and speed input
- Analog reference input
- RS232C/RS422 reference input
- Dynamic braking control for excess DC bus voltage
- Cycle-by-cycle on/off Control for Brake IGBT
- DC bus voltage feedback
- Standard Encoder interface with Hall ABC support
- A/B quadrature signal input up to 1 MHz
- Choice of separate or multiplexed Hall A/B/C signal input
- Auto-initialization with Hall A/B/C plus Z pulse input
- Adaptable for any line count encoder from 200 PPR to 10,000 PPR
- 1/T counter (1 MHz) for low speed performance improvement
- Space Vector PWM with deadtime insertion
- IR2175 current sensing IC interface
- IR213x high voltage gate driver IC interface
- Low cost serial 12 bit A/D interface with multiplexer and sample/hold circuit
- 4 channel analog output by PWM
0-3.3 V, 120 kHz output
- EEPROM for startup initialization of internal data/parameters through host register interface
AT24C01A, 128 x 8

- Versatile host communication interface
 - RS232C or RS422 host interface
 - Fast SPI slave host interface with multi-drop capability
 - Parallel Host interface (total 12 pins)
- Multiplexed data/address bus
 - Address Enable
 - RD/WR
- Discrete I/O
 - Start (Input)
 - Stop (Input)
 - IFBCAL (Input)
 - Fault Clear (Input)
 - Fault (Output)
 - SYNC (Output)
 - PWM Active (Output)
- LED
 - Two-bit bi-color

IRMCK201

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IRMCK201 Block Diagrams

Basic Block Diagram

Figure 1 shows the basic block diagram of the IRMCK201 surrounded by various Accelerator ICs. Host communications are provided over SPI, RS-232C or Host parallel ports. Two current sensing ICs (IR2175) and a three phase high voltage gate drive typically implement the high voltage / current interface between the IRMCK201 IC and motor.

The IRMCK201 can operate in a “stand-alone” mode without the host controller. A serial EEPROM could be utilized to load motor-specific parameters into the IC.

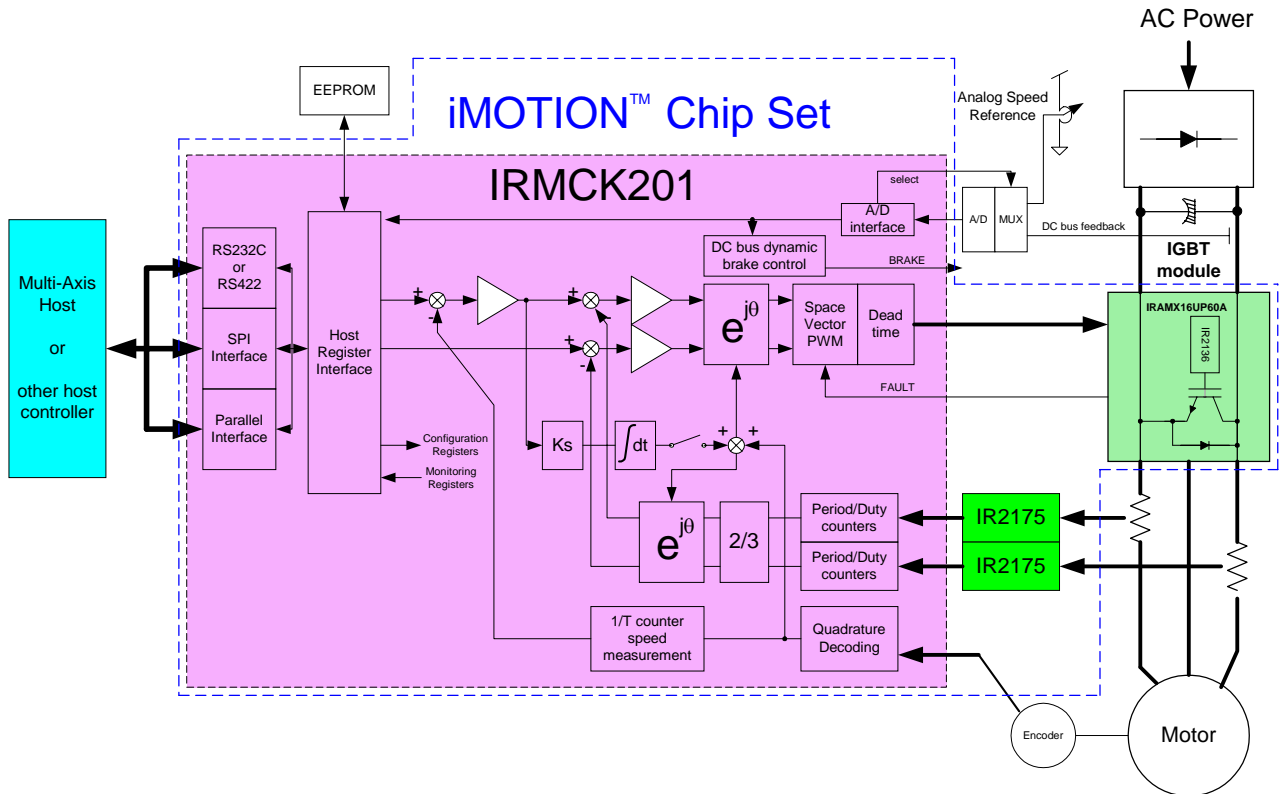


Figure 1. Basic Block Diagram of IRMCK201

IRMCK201

Detailed Block Diagram

Figure 2 shows a detailed block diagram of the IRMCK201. All logic and algorithms are pre-programmed, and the user does not need to make any effort to develop code, alleviating the tedious design process. If needed, the user can configure the drive to tailor the control per specific needs to meet the required specification. This configuration is easily done by accessing the host register set through the communication interface.

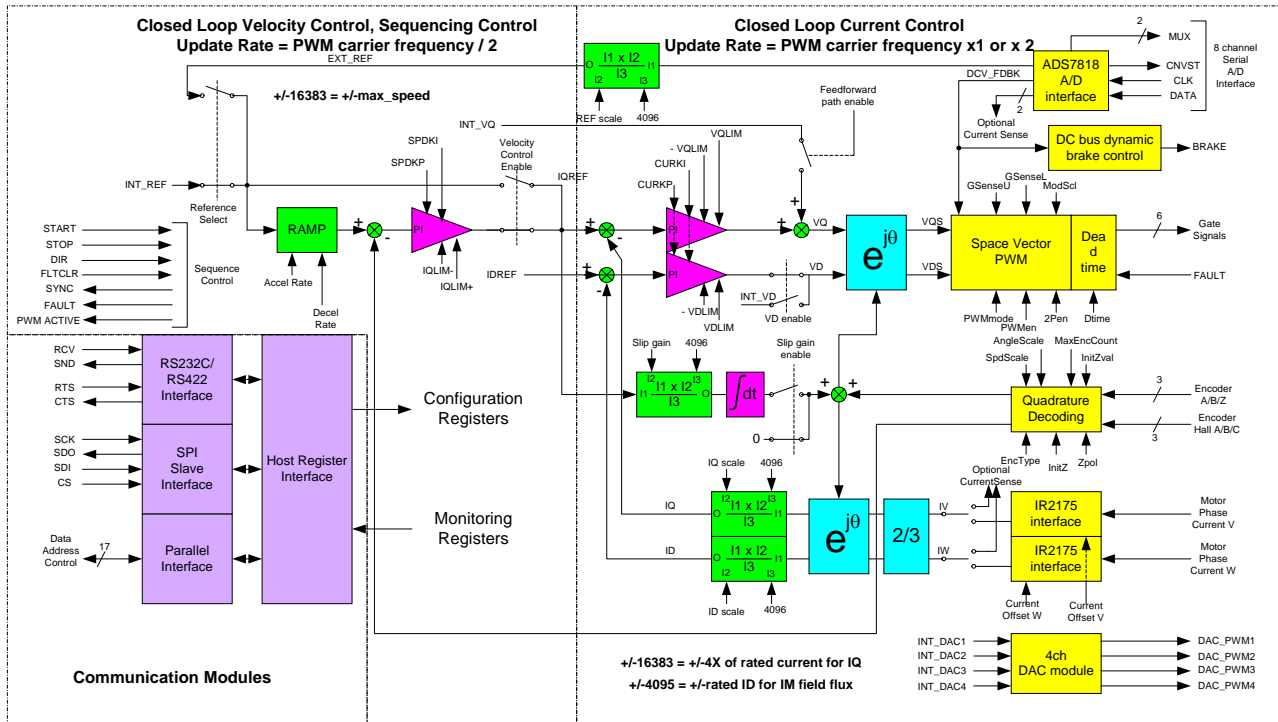


Figure 2. Detailed Block Diagram of IRMCK201

Input/Output of IRMCK201

Figure 3 shows the interface signals divided into sub-groups. For detailed pin assignment, please refer to Table 12 in this data sheet.

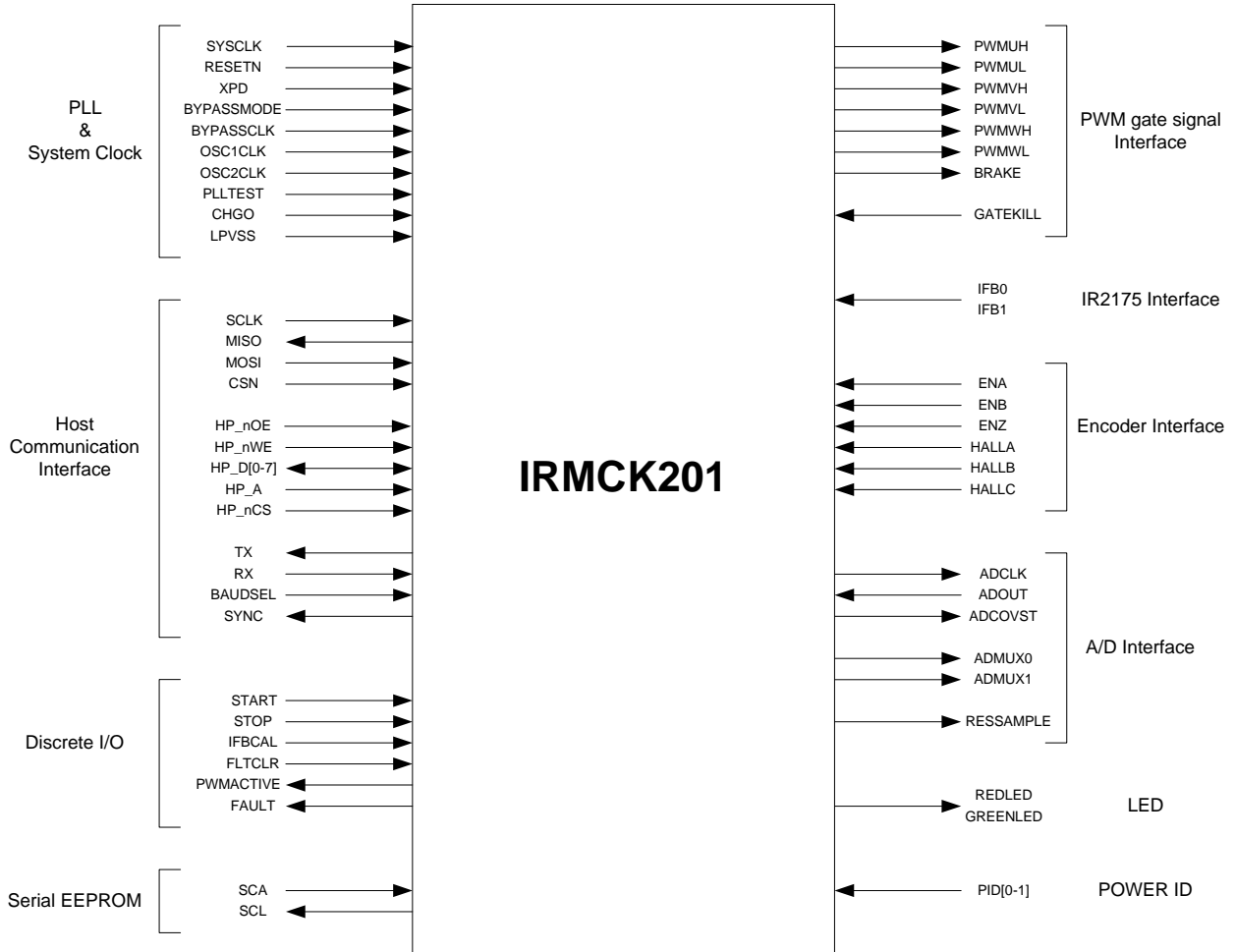


Figure 3. Input/Output of IRMCK201

IRMCK201

| Host Interface Group | | | |
|-----------------------------|-------------------------------|---|---|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| SCLK | I | Positive edge sensitive | SPI clock |
| MISO | O | - | Master input and slave output |
| MOSI | I | - | Master output and slave input |
| CSN | I | L | SPI chip select |
| HP_nOE | I | L | Parallel data output enable |
| HP_nWE | I | L | Parallel data write cycle identification |
| HP_D [7:0] | I/O | - | Parallel data |
| HP_A | I | H | Parallel data address cycle identification |
| HP_nCS | I | L | Chip select |
| TX | O | - | RS-232 data out |
| RX | I | - | RS-232 data in |
| BAUDSEL | I | H | RS-232 baud rate: 0 = 57,600; 1 = 1,031,250 bps |
| SYNC | O | L | Start of PWM cycle |

| Discrete I/O Group | | | |
|---------------------------|-------------------------------|---|-----------------------------------|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| IFBCAL | I | H | Current offset calibration signal |
| START | I | H | Start command |
| STOP | I | H | Stop command |
| FLTCLR | I | H | Fault clear command |
| PWMACTIVE | O | H | PWM state |
| FAULT | O | H | Fault state |

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| Motion Peripheral Group | | | |
|--------------------------------|-------------------------------|--|--|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| PWMUH | O | Varies, Based on Write Register 0x0D | PWM phase U high side |
| PWMUL | O | | PWM phase U low side |
| PWMVH | O | | PWM phase V high side |
| PWHVL | O | | PWM phase V low side |
| PWMWH | O | | PWM phase W high side |
| PWMWL | O | | PWM phase W low side |
| BRAKE | O | L | IGBT gate |
| GATEKILL | I | Varies, Based on Write Register 0x0C Bit 7 | When asserted, negates all six PWM signals, host writeable |
| IFB0 | I | - | Channel 0 (phase V) |
| IFB1 | I | - | Channel 1 (phase W) |
| ENA | I | - | Encoder A |
| ENB | I | - | Encoder B |
| ENZ | I | - | Encoder Z |
| HALLA | I | - | Hall A |
| HALLB | I | - | Hall B |
| HALLC | I | - | Hall C |

| Analog Interface Group | | | |
|-------------------------------|-------------------------------|---|-----------------------------|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| ADCLK | O | Negative Edge Sensitive | Clock to ADS7818 |
| ADOUT | I | - | Serial data from ADS7818 |
| DAC [3:0] | O | - | Diagnostic DAC |
| ADCONVST | O | L | Conversion start to ADS7818 |
| ADMUX0 | O | H | Analog input mux select |
| ADMUX1 | O | H | Analog input mux select |

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| PLL Interface Group | | | |
|---------------------|------------------------|----------------------------------|--|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| XPD | I | L | PLL reset |
| RESETN | I | L | Digital logic reset |
| BYPASSCLK | I | H | Internal test pin – force to logic low |
| BYPASSMODE | I | H | Internal test pin – force to logic low |
| OSC1CLK | I | - | 33.33 MHz crystal input |
| OSC2CLK | I | - | 33.33 MHz crystal input |
| PLLTEST | I | H | Internal test pin – force to logic low |
| CHGO | I/O | - | Low pass filter |
| LPVSS | I/O | - | Low pass filter ground |

| Miscellaneous Group | | | |
|---------------------|------------------------|--|--|
| Signal | Input (I) / Output (O) | Low (L) / High (H) True Asserted | Function |
| SD | O | Varies, Based on Write Register 0x0C Bit 1 | Shut down, host writeable |
| SCA | I/O | - | EEPROM data |
| SCL | O | Positive Edge Sensitive | EEPROM clock |
| PID[0:1] | I | - | Power ID to SystemStatus register, host readable |
| GREENLED | O | H | LED signal |
| REDLED | O | H | LED signal |

| Power Supply Group | |
|--------------------|--|
| Signal | Function |
| LVDD | IC Logic +3.3V power supply |
| AVCC | IC Analog +3.3V power supply |
| MVDD | IC Phase +3.3V Lock Loop power supply |
| VSSHCH | IC Phase Lock Loop power supply return |

Typical Application Connections

Typical application connection is shown in Figure 4. In order to complete a high performance servo drive control, all necessary components are shown in connection to IRMCK201.

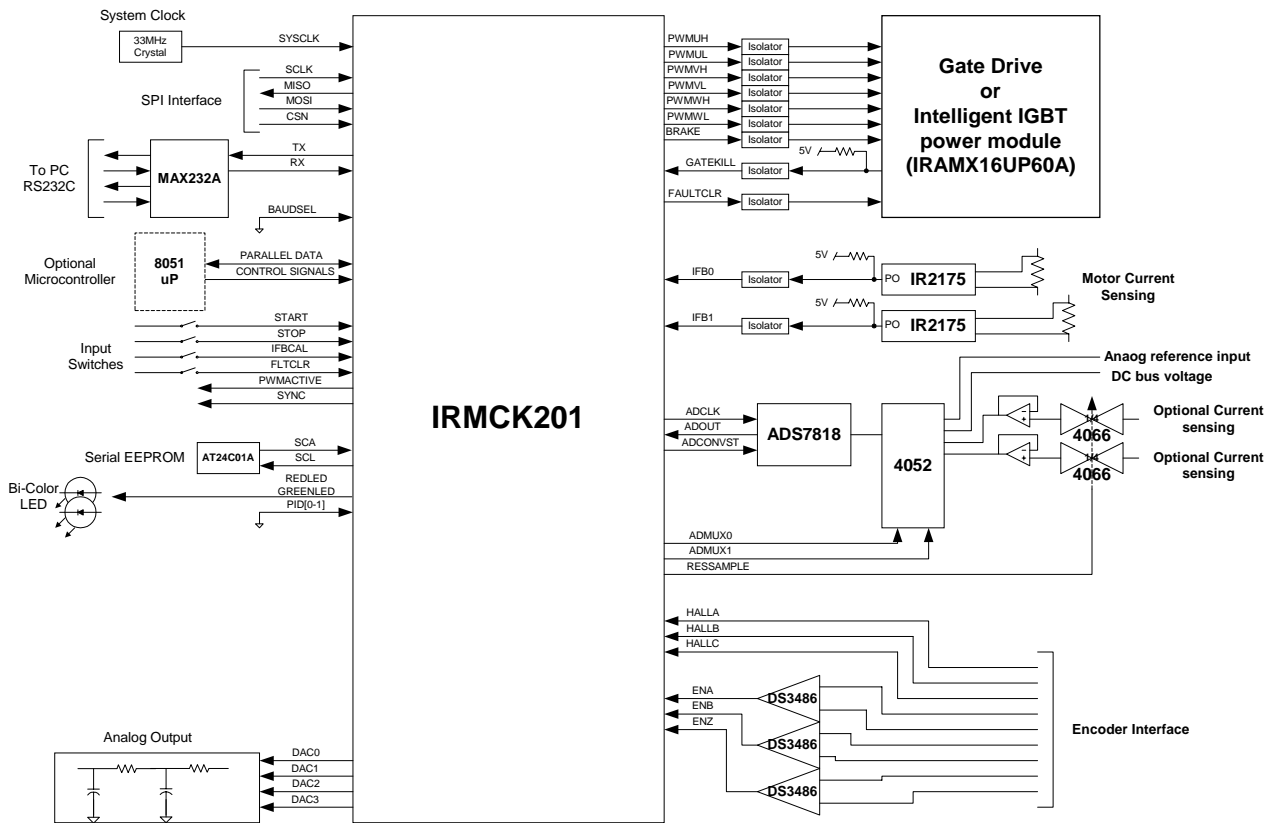


Figure 4. Typical Connection of IRMCK201

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IC Crystal Clock Circuitry

The clock input to the IC is a 33.33 MHz crystal oscillator. Two shunt capacitors and possibly a series resistor is required to terminate the crystal to the IC.

The values of the R/C will vary based on actual PCB attributes, and some empirical analysis may be required to get the PLL to start oscillating. Once oscillating, verify that the signal waveforms at the OSC1CLK and OSC2CLK pins are sinusoidal rather than trapezoidal. Refer to Table 1 for suggested R/C values. Most low-cost crystals can be used in this application. An example is a Citizen Part number CM309B33.333MABJT available from Digi-Key under part number 300-4160-1-ND.

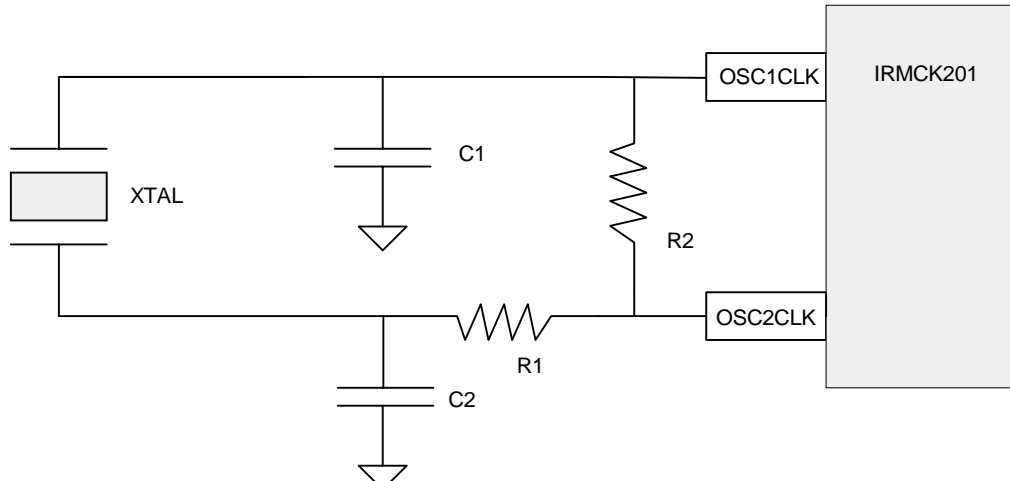


Figure 5. Oscillator Circuit

| Component | Value | Units |
|-----------|-------|----------|
| XTAL | 33.33 | MHz |
| C1 | 5 | pF |
| C2 | 5 | pF |
| R1 | 0 | Ω |
| R2 | 3.9K | Ω |

Table 1: Typical Values for the Clock Circuit

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PLL Clock Circuitry

The IRMCK201 contains a PLL that creates a 2X and 4X clock from the input 33.33 MHz input clock pin. There are a number of pins on the IC allocated for factory testing purposes, which need to be left unconnected. Table 2 shows required PCB signal connections for these pins. Note that N/C is for factory use only.

| Pin Number | PCB Connection |
|------------|----------------|
| 1 | VSS |
| 2 | VSS |
| 7 | VSS |
| 15 | N/C |
| 16 | N/C |
| 17 | N/C |
| 18 | N/C |
| 23 | N/C |
| 24 | N/C |
| 25 | N/C |
| 41 | N/C |
| 45 | N/C |
| 56 | N/C |
| 89 | N/C |

Table 2: PLL Test Pin Assignments

Low Pass Filter

The low pass filter for this PLL resides between the CHGO and LPVSS pins. Three passive components are required to implement this filter: C_p , R_p and C_s . Figure 6 shows how to place these components around the IC.

A shield should be placed below R_p , C_p and C_s made out of copper etch.

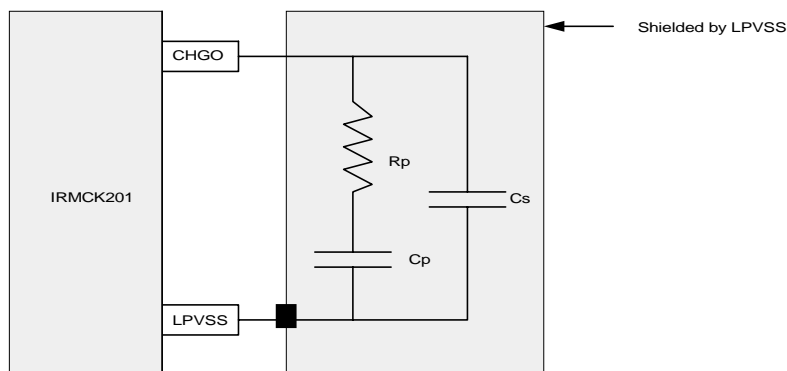


Figure 6. PLL Low Pass Filter Shielding

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Implementing the Low Pass Filter Shield

Make all connections between CHGO, Rp, Cp, Cs and LPVSS as short as possible. Create the underlining shield by “copper filling” a larger area in the signal plane of the PCB. Connect this shield to the LPVSS pin of the IC. Do not connect this shield to signal ground (VSS).

Cp Rp and Cs Component Values

For a typical FR4 PCB, the values of the passive components are shown in Table 3.

| Component | Value | Units |
|-----------|---------------|----------|
| Rp | 3.9K | Ω |
| Cp | 1000 | pF |
| Cs | Not Installed | - |

Table 3: PLL Low Pass Filter Values

PLL Reset

There are two reset pins on the IC, XPD and RESETN both low true. XPD holds the PLL circuitry in reset when low. Upon XPD going high, the PLL circuitry begins to lock onto the 33.33 MHz clock input. The PLL circuit may take up to 1 ms to become stable. RESETN asserted low holds the internal DSP logic in reset. Upon RESETN going high, the IC digital logic becomes active.

RESETN should be held low during and at least 1 ms after XPD goes high false to hold the internal DSP logic in reset while the PLL becomes stable.

DC Electrical Characteristics and Operating Conditions

Absolute Maximum Ratings

Note: VSS = 0 Volt

| PARAMETER | SYMBOL | LIMITS | UNIT S | NOTE |
|------------------------|--------|--------------------|--------|------------------------------|
| Power Supply Voltage | VDD | VSS-0.3 to 4.0 | V | |
| Input Voltage | VI | VSS-0.3 to VDD+0.5 | V | Non 5 Volt Tolerant Pins |
| | | VSS-0.3 to 7 | V | Only on 5 Volt Tolerant Pins |
| Output Voltage | VO | VSS-0.3 to VDD+0.5 | V | |
| Output Current per Pin | IOUT | +/- 30 | mA | |
| Storage Temperature | Tstg | -65 to 150 | °C | |

Table 4: Absolute Maximum Ratings

Recommended Operating Conditions

Note: VSS = 0 Volt

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTE |
|----------------------|--------|-----|-----|-----|-------|------------------------------|
| Power Supply Voltage | VDD | 3.0 | 3.3 | 3.6 | V | |
| Input Voltage | VI | VSS | - | VDD | V | Non 5 Volt Tolerant Pins |
| | | | | 5.5 | V | Only on 5 Volt Tolerant Pins |
| Ambient Temperature | Ta | -40 | - | 85 | °C | Note 1 |

Table 5: Recommended Operating Conditions

Notes:

- The ambient temperature range is recommended for $T_j = -40$ to 125 °C

IRMCK201

DC Characteristics

Common Quiescent and Leakage Current

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------|--------|---|-----|-----|------|-------|
| Quiescent Current | IDDS | VI=VDD or VSS VDD=MAX IOH=IOL=0 Ta=Tj=85°C | - | - | 0.35 | uA |
| Input Leakage Current | ILI | VDD=MAX VIH=VDD VIL=VSS | -1 | - | 1 | uA |

Table 6: DC Characteristics

Input Characteristics – Non Schmitt Trigger Inputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|--------|------------|-----|-----|-----|-------|
| High Level Input Voltage | VIH1 | VDD=MAX | 2.0 | - | - | V |
| Low Level Input Voltage | VIL1 | VDD=MIN | - | - | 0.8 | V |

Table 7: Non Schmitt Trigger Input Characteristics

Input Characteristics – Schmitt Trigger Inputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|--------|------------|-----|-----|-----|-------|
| High Level Input Voltage | VT1+ | VDD=MAX | 1.1 | - | 2.4 | V |
| Low Level Input Voltage | VT1- | VDD=MIN | 0.6 | - | 1.8 | V |
| Hysteresis Voltage | VH1 | VDD=MIN | 0.1 | - | - | V |

Table 8: Schmitt Trigger Input Characteristics

Output Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|--------|-----------------------|-----------|-----|-----------|-------|
| High Level Output Voltage | VOH3 | VDD=MIN IOH=-12mA | VDD - 0.4 | - | - | V |
| Low Level Output Voltage | VOL3 | VDD=MIN IOH = 12mA | - | - | VSS + 0.4 | V |

Table 9: Output Characteristics

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Output Characteristics OSC2CLK

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|--------|------------------------|-----------|-----|-----------|-------|
| High Level Output Voltage | LVOH | VDD=MIN IOH=-530uA | VDD - 0.4 | - | - | V |
| Low Level Output Voltage | LVOL | VDD=MIN IOH = 730uA | - | - | VSS + 0.4 | V |

Table 10: Output Characteristics OSC2CLK

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Pin and I/O Characteristic Table

| Pin Number | Pin Name | INTERNAL IC RESISTOR TERMINATION | Pin Type | 5.50 VOLT TOLERANT INPUT | INPUT DC CHARACTERISTIC TABLE | OUTPUT DC CHARACTERISTIC TABLE |
|------------|---------------|----------------------------------|----------|--------------------------|-------------------------------|--------------------------------|
| 1 | BYPASSMODE | 40K-240K Pull Down | I | - | Table 8 | - |
| 2 | BYPASSCLK | 40K-240K Pull Down | I | - | Table 8 | - |
| 3 | OSC1CLK | | I | - | Table 7 | - |
| 4 | LVDD | | P | - | - | - |
| 5 | OSC2CLK | | O | - | - | Table 11 |
| 6 | VSS | | P | - | - | - |
| 7 | PLLTEST | 20K-120K Pull Down | I | - | Table 7 | - |
| 8 | XPD | | I | - | Table 7 | - |
| 9 | VSSHC | | P | - | - | - |
| 10 | MVDD | | P | - | - | - |
| 11 | VSSHC | | P | - | - | - |
| 12 | AVDD | | P | - | - | - |
| 13 | CHGO | | O | - | - | - |
| 14 | LPVSS | | P | - | - | - |
| 15 | N.C. (CLKI) | | I | - | Table 8 | - |
| 16 | N.C. (CLKSEL) | | I | - | Table 8 | - |
| 17 | N.C. (CPT0) | | I | - | Table 8 | - |
| 18 | N.C. (CPT1) | | I | - | Table 8 | - |
| 19 | LVDD | | P | - | - | - |
| 20 | REDLED | | O | - | - | Table 9 |
| 21 | GREENLED | | O | - | - | Table 9 |
| 22 | VSS | | P | - | - | - |
| 23 | N.C. (TSTCLK) | | I | - | Table 8 | - |
| 24 | N.C. (TSTSEL) | | I | - | Table 8 | - |
| 25 | N.C. (OLAP) | | I | - | Table 8 | - |
| 26 | PWMWL | | O | - | - | Table 9 |
| 27 | PWMWH | | O | - | - | Table 9 |
| 28 | PWMVL | | O | - | - | Table 9 |
| 29 | LVDD | | P | - | - | - |
| 30 | PWMVH | | O | - | - | Table 9 |
| 31 | PWMUL | | O | - | - | Table 9 |
| 32 | VSS | | P | - | - | - |
| 33 | PWMUH | | O | - | - | Table 9 |
| 34 | BRAKE | | O | - | - | Table 9 |
| 35 | RESETN | 20K -120K Pull Up | I | - | Table 8 | - |
| 36 | FLTCLR | | O | - | - | Table 9 |
| 37 | GATEKILL | 20K -120K Pull Up | I | - | Table 8 | - |
| 38 | IFB0 | | I | YES | Table 8 | - |
| 39 | IFB1 | | I | YES | Table 8 | - |

IRMCK201

| Pin Number | Pin Name | INTERNAL IC RESISTOR TERMINATION | Pin Type | 5.50 VOLT TOLERANT INPUT | INPUT DC CHARACTERISTIC TABLE | OUTPUT DC CHARACTERISTIC TABLE |
|------------|-----------|----------------------------------|----------|--------------------------|-------------------------------|--------------------------------|
| 40 | SD | | O | - | - | Table 9 |
| 41 | N.C. (D0) | | I | - | Table 8 | - |
| 42 | PID0 | 20K -120K Pull Up | I | - | Table 8 | - |
| 43 | PID1 | 20K -120K Pull Up | I | - | Table 8 | - |
| 44 | LVDD | | P | - | - | - |
| 45 | N.C. (D3) | | I | - | Table 8 | - |
| 46 | CSN | | I | YES | Table 8 | - |
| 47 | VSS | | P | - | - | - |
| 48 | MOSI | | I | YES | Table 8 | - |
| 49 | MISO | | O | - | - | Table 9 |
| 50 | SCLK | | I | YES | Table 8 | - |
| 51 | TX | | O | - | - | Table 9 |
| 52 | RX | | I | YES | Table 8 | - |
| 53 | BAUDSEL | 20K -120K Pull Down | I | YES | Table 7 | - |
| 54 | LVDD | | P | - | - | - |
| 55 | ADMUX0 | | O | - | - | Table 9 |
| 56 | N.C. (N2) | | I | - | Table 8 | - |
| 57 | VSS | | P | - | - | - |
| 58 | ADMUX1 | | O | - | - | Table 9 |
| 59 | RESSAMPLE | | O | - | - | Table 9 |
| 60 | ADCONVST | | O | - | - | Table 9 |
| 61 | ADCLK | | O | - | - | Table 9 |
| 62 | ADOUT | | I | YES | Table 8 | - |
| 63 | SYNC | | O | - | - | Table 9 |
| 64 | FAULT | | O | - | - | Table 9 |
| 65 | START | 20K -120K Pull Down | I | YES | Table 8 | - |
| 66 | STOP | 20K -120K Pull Down | I | YES | Table 8 | - |
| 67 | IFBCAL | 20K -120K Pull Down | I | YES | Table 8 | - |
| 68 | FLTCLR | 20K -120K Pull Down | I | YES | Table 8 | - |
| 69 | LVDD | | P | - | - | - |
| 70 | PWMACTIVE | | O | - | - | Table 9 |
| 71 | DAC[3] | | O | - | - | Table 9 |
| 72 | VSS | | P | - | - | - |
| 73 | DAC[2] | | O | - | - | Table 9 |
| 74 | DAC[1] | | O | - | - | Table 9 |
| 75 | DAC[0] | | O | - | - | Table 9 |
| 76 | HP_D[0] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 77 | HP_D[1] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |

IRMCK201

| Pin Number | Pin Name | INTERNAL IC RESISTOR TERMINATION | Pin Type | 5.50 VOLT TOLERANT INPUT | INPUT DC CHARACTERISTIC TABLE | OUTPUT DC CHARACTERISTIC TABLE |
|------------|------------|----------------------------------|----------|--------------------------|-------------------------------|--------------------------------|
| 78 | HP_D[2] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 79 | VDD | | P | - | - | - |
| 80 | HP_D[3] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 81 | HP_D[4] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 82 | VSS | | P | - | - | - |
| 83 | HP_D[5] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 84 | HP_D[6] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 85 | HP_D[7] | 20K -120K Pull Down | B | - | Table 7 | Table 9 |
| 86 | HP_nOE | | I | YES | Table 8 | - |
| 87 | HP_nWE | | I | YES | Table 8 | - |
| 88 | HP_A | | I | YES | Table 8 | - |
| 89 | N.C. (N11) | | I | - | Table 8 | - |
| 90 | HP_nCS | | I | YES | Table 8 | - |
| 91 | ENCZ | | I | YES | Table 8 | - |
| 92 | ENCB | | I | YES | Table 8 | - |
| 93 | ENCA | | I | YES | Table 8 | - |
| 94 | LVDD | | P | - | - | - |
| 95 | HALLC | | I | YES | Table 8 | - |
| 96 | HALLB | | I | YES | Table 8 | - |
| 97 | VSS | | P | - | - | - |
| 98 | HALLA | | I | YES | Table 8 | - |
| 99 | SCL | | O | - | - | Table 9 |
| 100 | SDA | 20K -120K Pull Up | B | - | Table 7 | Table 9 |

Table 12: Pin and I/O Characteristics

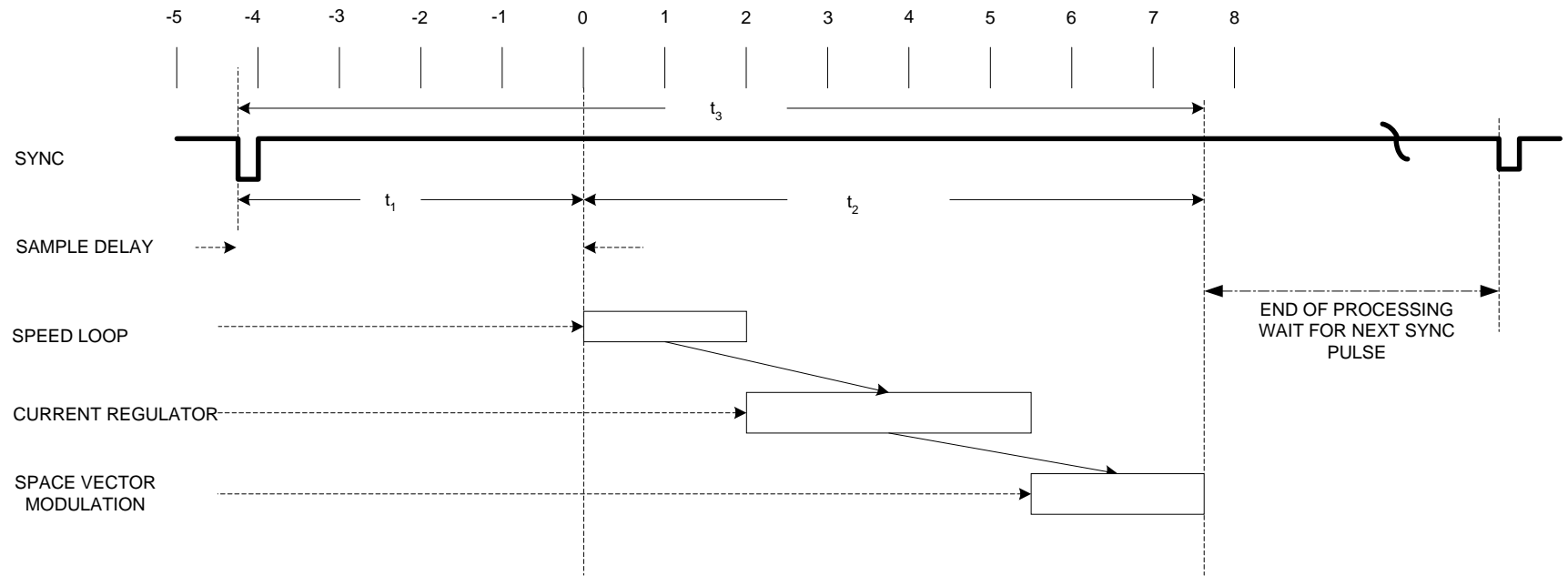
Power Consumption

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|--------|------------|-----|-------|-----|-------|
| P _{Total} | PTOTAL | VDD=3.3V | - | 0.927 | - | WATT |

Table 13: IRMCK201 Power Consumption

AC Electrical Characteristics and Operating Conditions

System Level AC Characteristics Sync Pulse to Sync Pulse Timing



Critical Path Timing Including PWM Calculation Time

Figure 7. System Level SYNC-to-SYNC Timing

| SYMBOL | DESCRIPTION | TIME | UNITS |
|--------|--|-------|---------------|
| t_1 | Current Feedback Sample Delay from SYNC Pulse Falling Edge | 4.32 | μs |
| t_2 | Closed Loop Computation Time (current control only including PWM computation) | 6.33 | μs |
| | Closed Loop Computation Time (current and velocity control including PWM calculation time) | 7.68 | |
| t_3 | Minimum SYNC-to-SYNC time (current control only including PWM calculation time) | 10.65 | μs |
| | Minimum SYNC-to-SYNC time (current and velocity control including PWM calculation time) | 12.0 | |

Table 14: System Level SYNC-to-SYNC Timing

FAULT and REDLED Response to GATEKILL

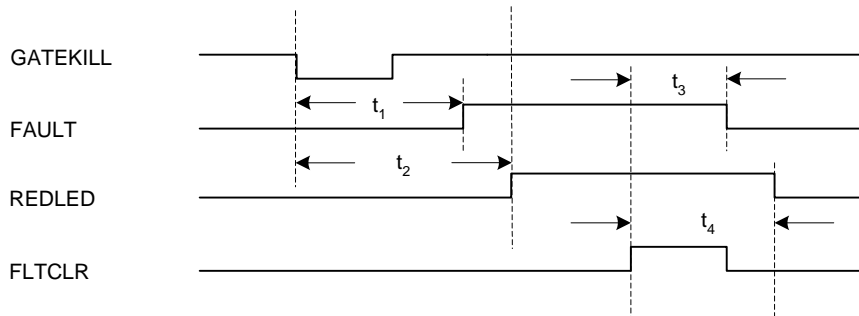


Figure 8. FAULT and REDLED Response to GATEKILL

| SYMBOL | DESCRIPTION | TYP | UNITS |
|--------|-----------------------------|-----|-------|
| t_1 | FAULT Response to GATEKILL | 685 | ns |
| t_2 | REDLED Response to GATEKILL | 715 | ns |
| t_3 | FAULT Response to FLTCLR | 145 | ns |
| t_4 | REDLED Response to FLTCLR | 175 | ns |

Table 15: FAULT and REDLED Response to GATEKILL

Host Interface AC Characteristics

SPI Timing

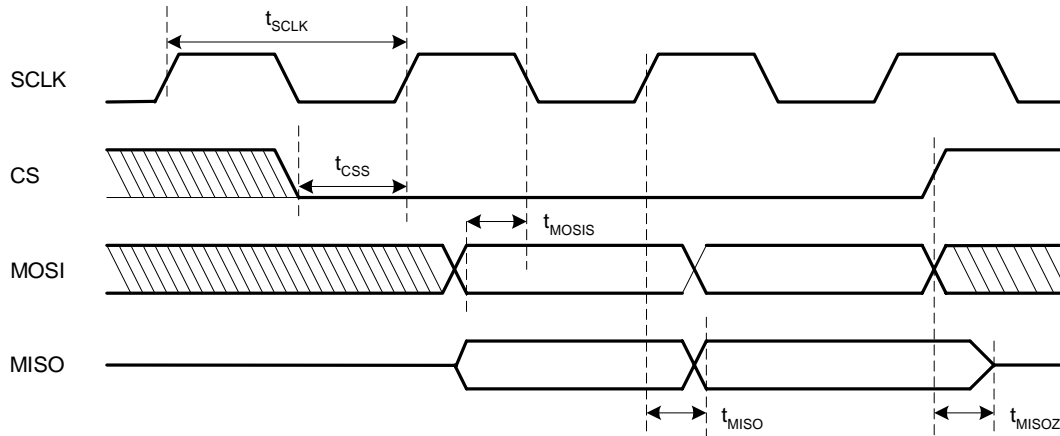


Figure 9. SPI Timing

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|-------------|---------------------------|-----|-----|-------|
| f_{SCLK} | ADC Clock Frequency | | 8 | MHz |
| t_{SCLK} | ADC Clock Period | 125 | | ns |
| t_{CSS} | CS to SCLK high Setup | 20 | | ns |
| t_{MOSIS} | MOSI to SCLK low Setup | 20 | | ns |
| t_{MISO} | SCLK to MISO Valid | 72 | | ns |
| t_{MIOZ} | CS to MISO High Impedance | 15 | 35 | ns |

Table 16: SPI Timing

Host Parallel Timing

Host Parallel Read Cycle

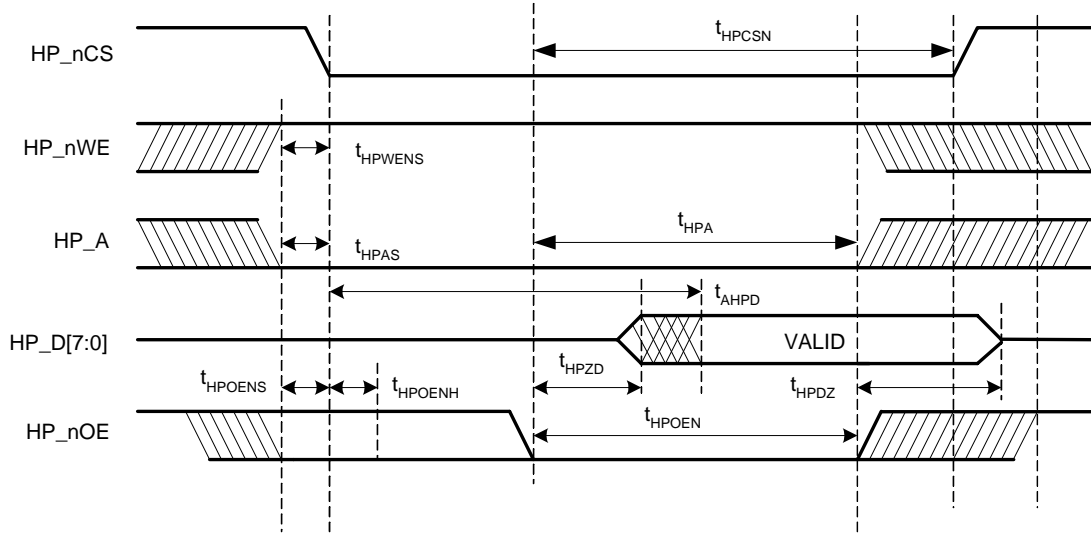


Figure 10. Host Parallel Read Cycle Timing

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT | NOTE |
|---------------------|---------------------------|-----|-----|------|--------|
| t _{HPCSN} | HP_nCS Period | 70 | | ns | |
| t _{HPWENS} | HP_nWE Setup | 10 | | ns | |
| t _{HPAS} | HP_A Setup | 10 | | ns | |
| t _{AHPD} | HP_D [7:0] Access | 60 | 105 | ns | |
| T _{HPZD} | HP_D [7:0] Active | 0 | 9 | ns | |
| t _{HPZ} | HP_D [7:0] High Impedance | 0 | 6 | ns | |
| t _{HPOENH} | HP_nOE Hold | 10 | | ns | Note 3 |
| t _{HPOENS} | HP_nOE Setup | 10 | | ns | Note 3 |
| t _{HPOEN} | HP_nOE Period | 70 | | ns | |

Table 17: Host Parallel Read Cycle Timing

Note:

- HP_nOE must be stable before and after the high to low transition of HP_nCS.

Host Parallel Write Cycle

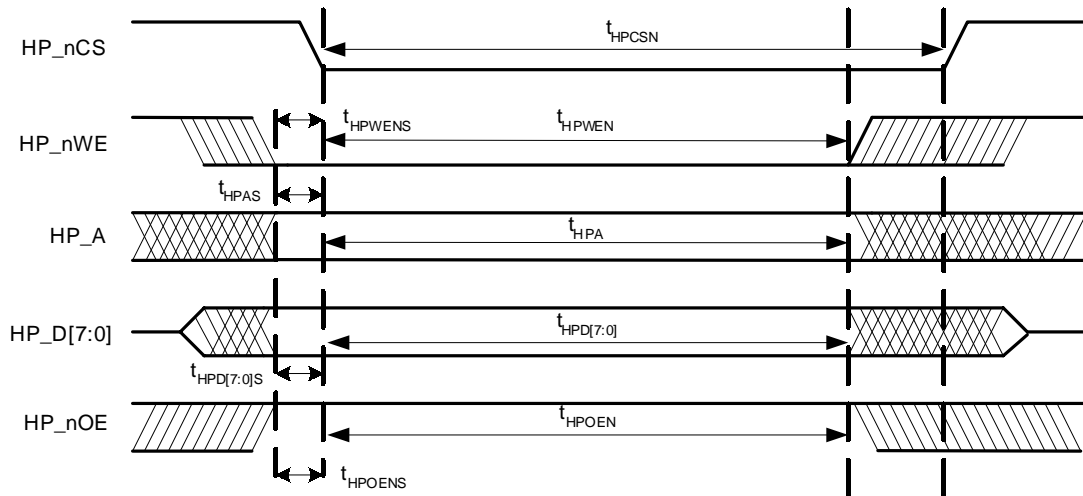


Figure 11. Host Parallel Write Cycle Timing

| SYMBOL | DESCRIPTION | MIN | UNITS | NOTE |
|-----------------------|------------------|-----|-------|--------|
| t_{HPCSN} | HP_nCS Period | 70 | ns | |
| t_{HPWENS} | HP_nWE Setup | 10 | ns | |
| t_{HPWEN} | HP_nWE Period | 70 | ns | |
| t_{HPAS} | HP_A Setup | -10 | ns | |
| t_{HPA} | HP_A Period | 70 | ns | |
| $t_{\text{HPD}[7:0]}$ | HP_D [7:0] Setup | -10 | ns | |
| t_{HPOENS} | HP_nOE Setup | 10 | ns | |
| t_{HPOEN} | HP_nOE Period | 70 | ns | Note 4 |

Table 18: Host Parallel Write Cycle Timing

Note:

- HP_nOE must be asserted high while HP_nCS low during a Host Parallel Write Cycle.

IRMCK201

Discrete I/O Electrical Characteristics

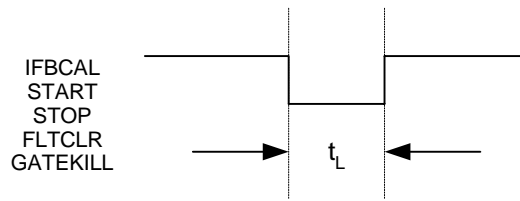


Figure 12. Discrete I/O Timing

| SYMBOL | DESCRIPTION | MIN | UNITS | NOTE |
|--------|----------------------|-----|-------|--------|
| t_L | Pulse Width IFBCAL | 100 | ms | |
| | Pulse Width START | 100 | ns | |
| | Pulse Width STOP | 100 | ns | |
| | Pulse Width FLTCLR | 1 | us | |
| | Pulse Width GATEKILL | 490 | ns | Note 5 |

Table 19: Discrete I/O Timing

Note:

- GATEKILL can be programmed to be low or high true. Shown above is a low true gate kill. The timing specification is the same.

IRMCK201

Motion Peripheral Electrical Characteristics

PWM Electrical Characteristics

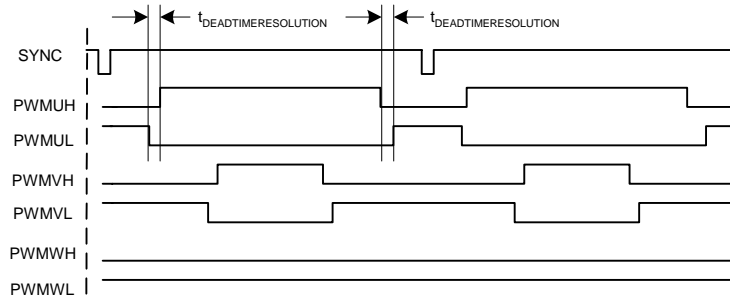


Figure 13. PWM Timing

| SYMBOL | DESCRIPTION | VALUE | UNITS |
|---------------------------------|-------------------------------------|-------|-------|
| $t_{\text{DEADTIMERESOLUTION}}$ | Deadtime Insertion Logic Resolution | 30 | ns |

Table 20: PWM Timing

IR2175 Interface

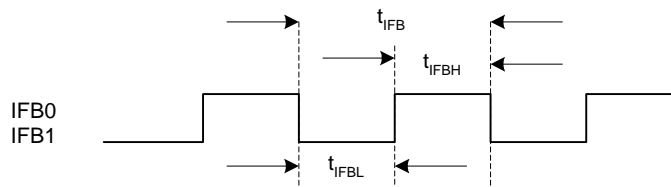


Figure 14. IR2175 Interface

| SYMBOL | DESCRIPTION | MIN | MAX | UNITS |
|-------------------|-----------------------------------|--------|------------------|---------------|
| f_{IFB} | Current Feedback Input Frequency | 95 | 165 | kHz |
| t_{IFB} | Current Feedback Period | 10.52 | 6.06 | μs |
| t_{IFBH} | Current Feedback High Pulse Width | 500 ns | 10 μs | |
| t_{IFBL} | Current Feedback Low Pulse Width | 500 ns | 10 μs | |

Table 21: IR2175 Interface

IRMCK201

Encoder Electrical Characteristics

Table 22 shows the input timing characteristics of the encoder inputs. Please refer to the IRMCK201 Application Developer's Guide for an example encoder input circuit that drives the IRMCK201.

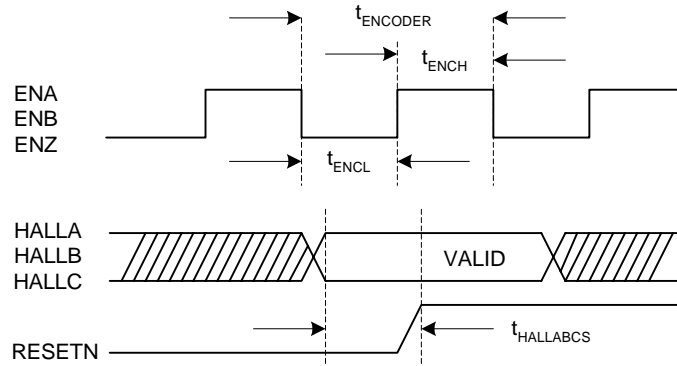


Figure 15. Encoder Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|-----------------------|-----------------------------------|-----|-----|-----|---------------|
| f_{ENCODER} | Encoder Input Frequency | | | 1 | MHz |
| t_{ENCODER} | ENA ENB ENZ Period | 1 | | | μs |
| t_{ENCL} | ENA ENB ENZ Pulse Width | 500 | | | ns |
| t_{ENCH} | ENA ENB ENZ Pulse Width | 500 | | | ns |
| t_{HALLABCS} | HALLA HALLB HALLC Setup to RESETN | 1 | | | μs |

Table 22: Encoder Timing

Analog To Digital Interface Electrical Characteristics

ADC Timing

System Level Timing

The IRMCK201 contains logic to drive an ADC Converter, Analog MUX and associated Sample and Hold circuits. Figure 16 and Table 23 show the system level timing of these elements. Figure 17 and Table 24 show specific timing parameters associated with the ADC Converter. Refer to the Application Developers Guide for a detailed description of ADC, MUX and Sample and Hold signal system level protocol. The IRMCK201 ADC interface has been designed for interfacing to the Burr-Brown ADS7818 ADC and Texas Instruments CD4052 MUX.

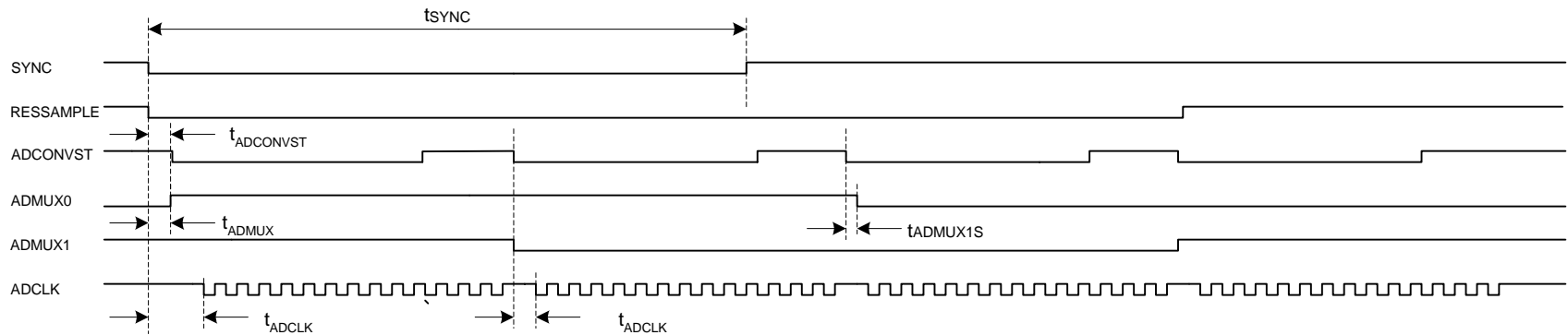


Figure 16. Top Level ADC Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|------------------|--------------------------------------|-----|-----|-----|---------|
| t_{SYNC} | SYNC Pulse Width | | 3 | | μs |
| $t_{RESSAMPLES}$ | SYNC Falling Edge to RESSAMPLE Valid | -10 | | 10 | ns |
| $t_{ADMUX0S}$ | ADCONVST to ADMUX0 Valid | 40 | | 61 | ns |
| $t_{ADMUX1S}$ | ADCONVST to ADMUX1 Valid | 40 | | 61 | ns |
| $t_{ADCONVSTS}$ | ADCONVST to ADCLK | 71 | | 91 | ns |

Table 23: Top Level ADC Timing

IRMCK201

Converter Level Timing

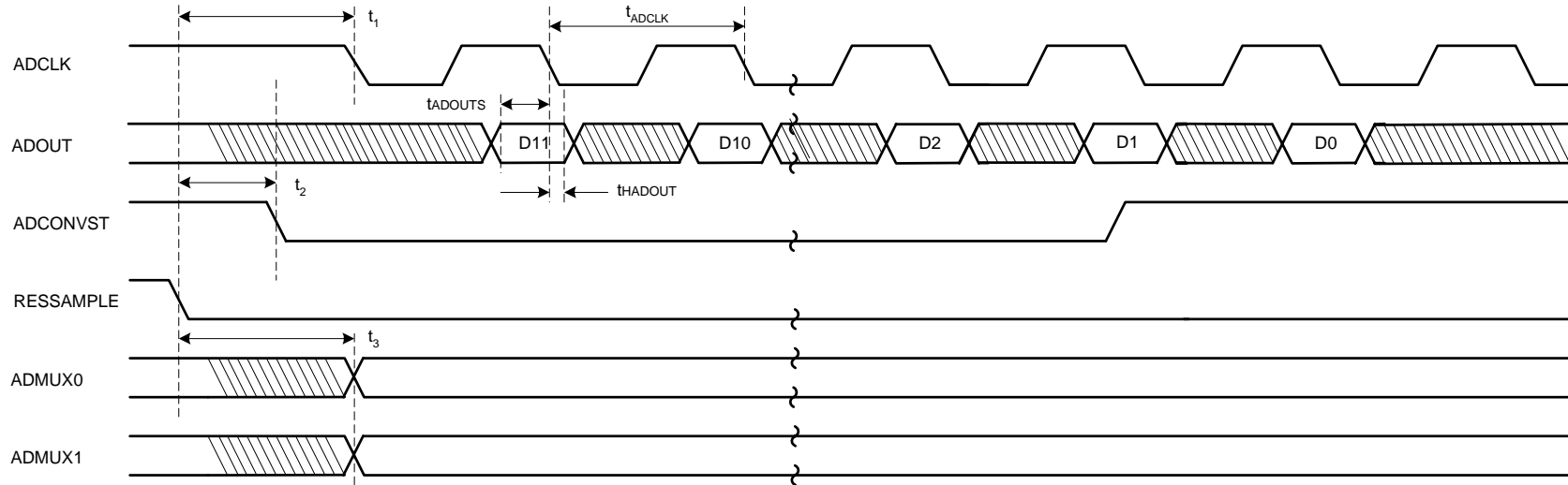


Figure 17. ADC Specific Timing

| SYMBOL | DESCRIPTION | VALUE | MIN | MAX | UNITS |
|--------------|-----------------------------|-------|------|-----|-------|
| f_{ADCLK} | ADC Clock Frequency | 8.33 | | | MHz |
| t_{ADCLK} | ADC Clock Period | 120 | | | ns |
| t_1 | RESSAMPLE to ADCLK | | | 91 | ns |
| t_2 | RESSAMPLE to ADCONVST | | | 40 | ns |
| t_3 | RESSAMPLE to ADMUX0, ADMUX1 | | | 64 | ns |
| T_{ADOUTS} | ADOUT to ADCLK Setup | | 19.7 | | |
| T_{HADOUT} | ADOUT to ADCLK Hold | | 2 | | ns |

Table 24: ADC Specific Timing

PLL Interface Electrical Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|-------------------|---------------------------------|------|-----|------|---------|
| Current Consumption | IDDS | Static | - | - | 170 | μ A |
| Current Consumption | IDD | Dynamic | - | 5 | - | mA |
| Peak jitter | T _{pj} | - | - | - | 1000 | ps |
| Cycle jitter | T _{cj} | - | -500 | - | +500 | ps |
| Lock-up Time | T _{lock} | - | - | - | 1 | ms |
| PLL Reset Period | Trst | Recommended operating condition | 10 | - | - | ns |

Table 25: PLL Electrical Characteristics

Appendix A Host Register Map

A host computer controls the IRMCK201 using its slave-mode Full-Duplex SPI port, a standard RS-232 port or a 8-bit parallel port for connection to a microprocessor. All interfaces are always active and can be used interchangeably, although not simultaneously. Control/status registers are mapped into a 128-byte address space.

Host Parallel Access

The IRMCK201 contains an address register that is updated with the Host Register address when HP_A = 1. After each subsequent data byte is either read or written, the internal address register is incremented. The diagram below shows that Data Bytes 0 to N would access register locations initially specified by the Address Byte. The Address Byte with the HP_A signal can be asserted at any time.

| | | | |
|--------------------------|-------------------------|-------------------|-------------------------|
| Address Byte HP_A = 1 | Data Byte 0 HP_A = 0 | HP_A = 0 | Data Byte N HP_A = 0 |
|--------------------------|-------------------------|-------------------|-------------------------|

Host Parallel Data Transfer Format

SPI Register Access

When configured as an SPI device read only and read/write operations are performed using the following transfer format:

| | | | |
|--------------|-------------|-------|-------------|
| Command Byte | Data Byte 0 | | Data Byte N |
|--------------|-------------|-------|-------------|

Data Transfer Format

| Bit Position | | | | | | | |
|--------------|-------------------------------|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Read Only | Register Map Starting Address | | | | | | |

Command Byte Format

Data transfers begin at the address specified in the command byte and proceed sequentially until the SPI transfer completes. As in the Host Parallel Access, the internal address register is incremented after each SPI byte is transferred. Note that accesses are read/write unless the “read only” bit is set.

RS-232 Register Access

The IRMCK201 includes an RS-232 interface channel that allows operation using a direct connection to the host PC. This interface implements a simple protocol that checks the validity of data prior to being written into a register. The protocol is explained below.

RS-232 Register Write Access

IRMCK201

A Register write operation consists of a command/address byte, byte count, register data and checksum. When the IRMCK201 receives the register data, it validates the checksum, writes the register data, and transmits an acknowledgement to the host.

| | | | |
|------------------------|------------|----------------------------|----------|
| Command / Address Byte | Byte Count | 1-6 bytes of register data | Checksum |
|------------------------|------------|----------------------------|----------|

Register Write Operation

| | |
|------------------------------|----------|
| Command Acknowledgement Byte | Checksum |
|------------------------------|----------|

Register Write Acknowledgement

| Bit Position | | | | | | | |
|--------------------|-------------------------------|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1=Read/ 0=Write | Register Map Starting Address | | | | | | |

Command/Address Byte Format

| Bit Position | | | | | | | |
|------------------|-------------------------------|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1=Error/ 0=OK | Register Map Starting Address | | | | | | |

Command Acknowledgement Byte Format

The following example shows a command sequence sent from the host to the IRMCK201 requesting a two-byte register write operation:

- 0x2F Write operation beginning at offset 0x2F
- 0x02 Byte count of register data is 2
- 0x00 Data byte 1
- 0x04 Data byte 2
- 0x35 Checksum (sum of preceding bytes, overflow discarded)

A good reply from the IRMCK201 would appear as follows:

- 0x2F Write completed OK at offset 0x2F
- 0x2F Checksum

An error reply to the command would have the following format:

- 0xAF Write at offset 0x2F completed in error
- 0xAF Checksum

RS-232 Register Read Access

A register read operation consists of a command/address byte, byte count and checksum. When the IRMCK201 receives the command, it validates the checksum and transmits the register data to the host.

IRMCK201

| | | |
|------------------------|------------|----------|
| Command / Address Byte | Byte Count | Checksum |
|------------------------|------------|----------|

Register Read Operation

| | | |
|------------------------------|----------------------------------|----------|
| Command Acknowledgement Byte | Register Data (Byte Count bytes) | Checksum |
|------------------------------|----------------------------------|----------|

Register Read Acknowledgement (transfer OK)

| | |
|------------------------------|----------|
| Command Acknowledgement Byte | Checksum |
|------------------------------|----------|

Register Read Acknowledgement (error)

The following example shows a command sequence sent from the host to the IRMCK201 requesting four bytes of read register data:

```
0xA0    Read operation beginning at offset 0x20 (high-order bit selects read operation)
0x04    Requested data byte count is 4
0xA4    Checksum
```

A good reply from the IRMCK201 might appear as follows:

```
0x20    Read completed OK at offset 0x20
0x11    Data byte 1
0x22    Data byte 2
0x33    Data byte 3
0x44    Data byte 4
0xCA    Checksum
```

An error reply to the command would have the following format:

```
0xA0    Read at offset 0x20 completed in error
0xA0    Checksum
```

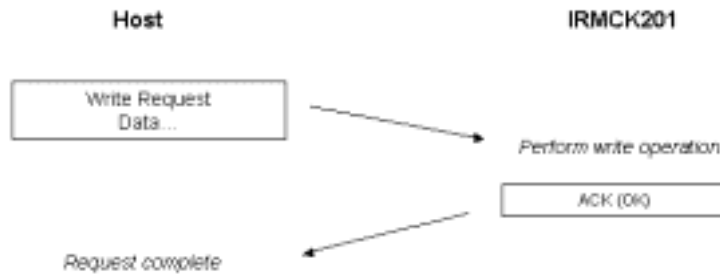
RS-232 Timeout

The IRMCK201 receiver includes a timer that automatically terminates transfers from the host to the IRMCK201 after a period of 32 msec.

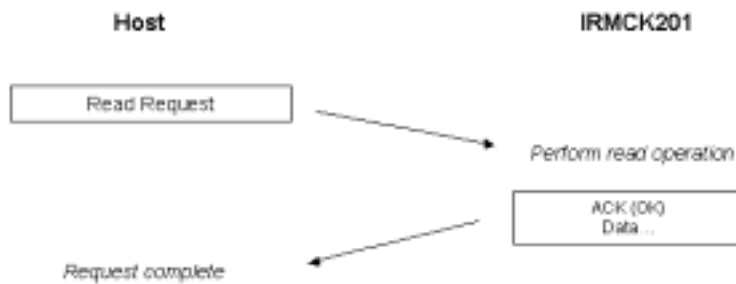
RS-232 Transfer Examples

The following example shows a normal exchange executing a register write access.

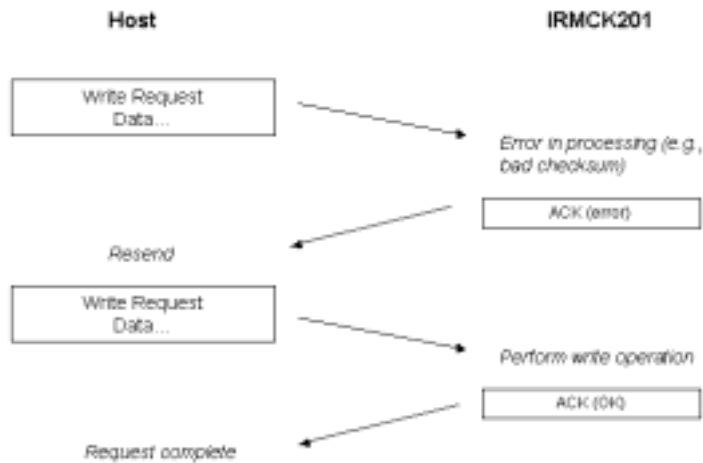
IRMCK201



The example below shows a normal register read access exchange.

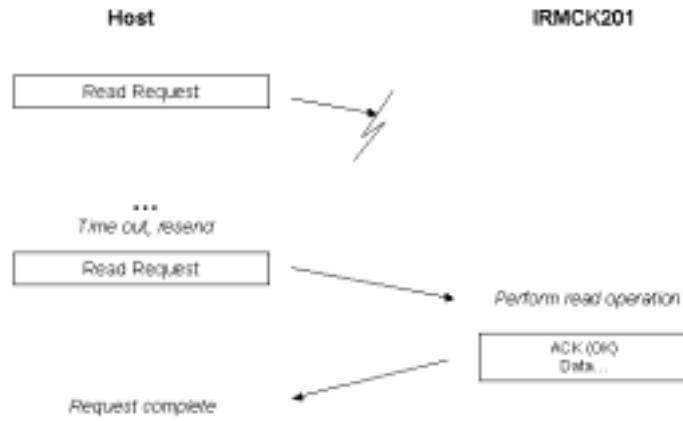


The following example shows a register write request that is repeated by the host due to a negative acknowledgement from the IRMCK201.



In the final example, the host repeats a register read access request when it receives no response to its first attempt.

IRMCK201



Write Register Definitions

QuadratureDecode Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|-------------------------|---|---|---------------|------------------------|----------------------|------------------|---------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 | EncCntW (LSBs) (W) | | | | | | | |
| 0x1 | EncCntW (MSBs) (W) | | | | | | | |
| 0x3 | MaxEncCnt (LSBs) (W) | | | | | | | |
| 0x4 | MaxEncCnt (MSBs) (W) | | | | | | | |
| 0x6 | ZEncCnt (LSBs) (W) | | | | | | | |
| 0x7 | ZEncCnt (MSBs) (W) | | | | | | | |
| 0x9 | EncAngScl (LSBs) (W) | | | | | | | |
| 0xA | EncAngScl (MSBs) (W) | | | | | | | |
| 0xB | SPARE | | | RedSig (W) | PwrOn RedSig (W) | ZPulse Enb (W) | ZPulsePol (W) | CntEnb (W) |

QuadratureDecode Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| EncCntW | W | New value for 16-bit Quadrature Decoder counter. |
| MaxEncCnt | W | Maximum value of 16-bit Quadrature Decoder counter. The encoder count is reset to 0 after this count has been reached. This maximum should be set to correspond to a 360-degree physical angle. |
| ZEncCnt | W | Encoder count value when the Z-pulse occurs. This value is loaded automatically in hardware when the Z-pulse occurs. (See ZPulseEnb and ZPulsePol fields below.) |

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| Field Name | Access (R/W) | Field Description |
|-------------|--------------|---|
| EncAngScl | W | This value should be set to $((MtrPoles / 2) * (4096 * 4096) / (MaxEncCnt + 1))$, where MtrPoles is the number of motor poles. The value is used to convert the encoder count to an angle ranging from 0 - 4095 using the equation: Angle = $((MtrPoles / 2) * 4096 * (encoder\ count) / (MaxEncCnt + 1)) \text{ MOD } 4096$. (The current encoder count can be read from the EncCntR field of the QuadratureDecodeStatus read register group.) |
| CntEnb | W | Encoder counter enable. |
| ZPulsePol | W | ZPULSE polarity. 1= load ZEncCnt on rising Z-pulse edge. 0= load ZEncCnt on falling Z-pulse edge. |
| ZPulseEnb | W | ZPULSE count initialization enable. When this bit is set, the encoder count is set to the ZEncCnt value at each Z-pulse edge as determined by the ZPulsePol field. |
| PwrOnRedSig | W | PowerOn Reduced signal enable. Set this bit in the EEPROM to enable EEPROM standalone initialization for a wire-saving encoder. When this bit is set, the EEPROM initialization uses the PwrOnHallA, PwrOnHallB, PwrOnHallC bits instead of the HallA, HallB, HallC bits to determine initial motor angle. (The Hall bits can be read from the QuadratureDecodeStatus read register group.) |
| RedSig | W | Reduced signal encoder enable. 1 = read Hall A/B/C fields from encoder A/B/Z wires. |

QuadratureDecode Write Register Field Definitions

PwmConfig Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|----------------------|-------|---------------|---------------|----------------------|---|--------|-------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xC | Gatekill Sns (W) | SPARE | Gate SnsL (W) | Gate SnsU (W) | SPARE | | SD (W) | SPARE |
| 0xD | PwmPeriod (LSBs) (W) | | | | | | | |
| 0xE | SPARE | | PwmConfig (W) | | PwmPeriod (MSBs) (W) | | | |
| 0xF | PwmDeadTm (W) | | | | | | | |

PwmConfig Write Register Map

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| Field Name | Access (R/W) | Field Description |
|-------------|--------------|--|
| SD | W | Shutdown control output to IR213x. |
| GateSnsU | W | Upper IGBT gate sense. 1 = active high gate control, 0 = active low gate control. |
| GateSnsL | W | Lower IGBT gate sense. 1 = active high gate control, 0 = active low gate control. |
| GatekillSns | W | GATEKILL signal sense. 1 = active high GATEKILL, 0 = active low GATEKILL. |
| PwmPeriod | W | This field is used to set the desired PWM frequency using the following equation: $\text{PwmPeriod} = 33,333,000 / (2 * (\text{PWM frequency})) - 1,$ where 33,333,000 is the system clock frequency (33.333MHz). Note that while "PwmPeriod" is the name of this field, the actual PWM carrier period is $2 * (\text{PwmPeriod} + 1) * (\text{System Clock Period} = 30\text{ns})$. |
| PwmConfig | W | PWM Configuration. 0 = Asymmetrical center aligned PWM, 1 = Symmetrical Center aligned PWM. |
| PwmDeadTm | W | Gate drive dead time in units of system clock cycles (e.g., 30 ns with 33 MHz clock). |

PwmConfig Write Register Field Definitions

CurrentFeedbackConfig Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|------------------------|---|---|---|------------------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x10 | IfbOffsV (LSBs) (W) | | | | | | | |
| 0x11 | IfbOffsW (LSBs) (W) | | | | IfbOffsV (MSBs) (W) | | | |
| 0x12 | IfbOffsW (MSBs) (W) | | | | | | | |
| 0x13 | IdScl (LSB) (W) | | | | | | | |
| 0x14 | IdScl (MSB) (W) | | | | | | | |
| 0x15 | IqScl (LSB) (W) | | | | | | | |
| 0x16 | IqScl (MSB) (W) | | | | | | | |

CurrentFeedbackConfig Write Register Map

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| IfbOffsV | W | 12-bit signed value for V phase current feedback offset. When the IfbOffsEnb bit in the SystemControl write register group is "0" this value is automatically added to each current measurement in hardware. |
| IfbOffsW | W | 12-bit signed value for W phase current feedback offset. When the IfbOffsEnb bit in the SystemControl write register group is "0" this value is automatically added to each current measurement in hardware. |
| IdScl | W | Rotating frame Id component current feedback scale factor. Constant used to scale current measurements before they are used in the field orientation calculation. This is a 15-bit fixed-point signed number with 10 fractional bits that ranges from $-16 + 1023 / 1024$. |
| IqScl | W | Rotating frame Iq component current feedback scale factor. Constant used to scale current measurements before they are used in the field orientation calculation. This is a 15-bit fixed-point signed number with 10 fractional bits that ranges from $-16 + 1023 / 1024$. |

CurrentFeedbackConfig Write Register Field Definitions

SystemControl Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|-------------|-------|---|---|----------|----------|----------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x17 | DcComp Enb | IfbOffs Enb | SPARE | | | Reserved | Foc EnbW | Pwm EnbW |

SystemControl Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|--|
| PwmEnbW | W | PWM Enable bit. Setting this bit to 1 or 0 sets the IGBT gate control signals to their active or inactive states. At power up the gate control output signals remain in a high-Z state. After PwmEnbW is set for the first time, the gate controls are driven to their active or inactive states according to the value of PwmEnbW. A fault condition clears this bit automatically in hardware. |
| FocEnbW | W | Field Orientated Control Enable bit. Setting this bit to 1 enables the FOC algorithm. Setting this bit to 0 resets the FOC algorithm and causes zero output voltage to be applied to the motor. A fault condition clears this bit automatically in hardware. |
| Reserved | W | This field should be reserved and should be set to 0. |

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| IfbOffsEnb | W | When IFB PwmEnbW = 1, and FocEnbW = 0, the Current feedback offset is calculated and saved in the CurrentFeedbackOffset read register group. When IfbOffsEnb = 1, the Current feedback offset values in the CurrentFeedbackOffset Read registers are applied to each current feedback measurement. When IfbOffsEnb = 0, the Current feedback offset values in the CurrentFeedbackConfig Write registers are applied to each current feedback measurement. |
| DcCompEnb | W | DC Bus Compensation enable. When this bit is set to "1", PWM output is compensated for using the following formula: $\text{PWM (comp)} = \text{PWM} * 310 / \text{DCBUSVOLTS}$ where PWM (comp) is the compensated PWM output voltage; PWM is the uncompensated PWM output voltage; 310 is the nominal DC bus voltage; and DCBUSVOLTS is the actual DC bus voltage. |

SystemControl Write Register Field Definitions

CurrentLoopConfig Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x18 | IqRefW – Quadrature Reference Current (LSBs) (W) | | | | | | | |
| 0x19 | IqRefW – Quadrature Reference Current (MSBs) (W) | | | | | | | |
| 0x1A | Kplreg – Current Loop Proportional Gain (LSBs) (W) | | | | | | | |
| 0x1B | Kplreg – Current Loop Proportional Gain (MSBs) (W) | | | | | | | |
| 0x1C | Kxlreg – Current Loop Integral Gain (LSBs) (W) | | | | | | | |
| 0x1D | Kxlreg – Current Loop Integral Gain (MSBs) (W) | | | | | | | |
| 0x1E | IdRef – Direct/Magnetizing Reference Current (LSBs) (W) | | | | | | | |
| 0x1F | IdRef – Direct/Magnetizing Reference Current (MSBs) (W) | | | | | | | |
| 0x20 | SlipGn (LSBs) (W) | | | | | | | |
| 0x21 | SlipGn (MSBs) (W) | | | | | | | |
| 0x22 | VqLim – Quadrature Current Output Limit (LSBs) (W) | | | | | | | |
| 0x23 | VqLim – Quadrature Current Output Limit (MSBs) (W) | | | | | | | |

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| Byte Offset | Bit Position | | | | | | | |
|-------------|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x26 | VdLim – Direct Current Output Limit (LSBs) (W) | | | | | | | |
| 0x27 | VdLim – Direct Current Output Limit (MSBs) (W) | | | | | | | |

CurrentLoopConfig Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| IqRefW | W | 15-bit signed quadrature current reference input from velocity loop. |
| Kplreg | W | 15-bit signed current loop PI controller proportional gain. Scaled with 14 fractional bits for an effective range of 0 – 1. |
| Kxlreg | W | 15-bit signed current loop PI controller integral gain. Scaled with 19 fractional bits for an effective range of 0 - .03125. |
| IdRef | W | 15-bit signed direct/magnetized current to D-axis current loop PI controller. |
| SlipGn | W | This parameter controls the slip speed for induction motor applications. SlipGn should be set to $2048 * 2048 * (\text{Rated slip speed in Hz}) / (\text{Current loop update frequency})$. SlipGn MUST be set to 0 if slip is not desired. |
| VqLim | W | 16-bit Quadrature current PI controller voltage output limit. |
| VdLim | W | 16-bit Direct current PI controller voltage output limit. |

CurrentLoopConfig Write Register Field Definitions

VelocityControl Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--|---|---|---|-----------|---|---|----------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x31 | SPARE | | | | SpdLpRate | | | SpdLpEnb |
| 0x32 | KpSreg – Velocity loop proportional gain (LSBs) (W) | | | | | | | |
| 0x33 | KpSreg – Velocity loop proportional gain (MSBs) (W) | | | | | | | |
| 0x34 | KxSreg – Velocity loop integral gain (LSBs) (W) | | | | | | | |
| 0x35 | KxSreg – Velocity loop integral gain (MSBs) (W) | | | | | | | |
| 0x36 | SregLimP – Velocity loop positive Limit (LSBs) (W) | | | | | | | |
| 0x37 | SregLimP – Velocity loop positive Limit (MSBs) (W) | | | | | | | |

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| Byte Offset | Bit Position | | | | | | | |
|-------------|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x38 | SregLimN – Velocity loop negative Limit (LSBs) (W) | | | | | | | |
| 0x39 | SregLimN – Velocity loop negative Limit (MSBs) (W) | | | | | | | |
| 0x3A | SpdScl – Speed Scale Factor (LSBs) | | | | | | | |
| 0x3B | SpdScl – Speed Scale Factor (MSBs) | | | | | | | |
| 0x3C | TargetSpd – Setpoint/target speed (LSBs) | | | | | | | |
| 0x3D | TargetSpd – Setpoint/target speed (MSBs) | | | | | | | |
| 0x3E | SpdAccRate – Acceleration | | | | | | | |
| 0x3F | SpdDecRate – Deceleration | | | | | | | |

VelocityControl Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| SpdLpEnb | W | Speed loop enable: 1 = enable speed loop PI controller. 0 = Reset Speed loop PI controller. |
| SpdLpRate | W | Speed loop update rate: 0 = disabled, N = update speed loop immediately before every Nth current loop update. |
| KpSreg | W | 15-bit velocity loop proportional gain, in fixed point with 5 fractional bits. Range = 0 - 512. |
| KxSreg | W | 15-bit velocity loop integral gain, in fixed point with 13 fractional bits. Range = 0 - 2. |
| SregLimP | W | 16-bit speed PI controller output positive limit. |
| SregLimN | W | 16-bit speed PI controller output negative limit (2's complement). |
| SpdScl | W | Motor Speed Scale factor. The user should set $SpdScl = 60 * 16383 * (33.333MHz/32) / (Max\ RPM * Encoder\ PPR) / 2$, which will result in a Speed value ranging ± 16384 corresponding to $\pm Max\ RPM$. |
| TargetSpd | W | Velocity loop speed setpoint in SPEED units, which are determined by the user via the SpdScl register setting. |
| SpdAccRate | W | Velocity loop acceleration in units of SPEED / Velocity loop execution or SPEED / (SpdLpRate / PWM period). |
| SpdDecRate | W | Velocity loop deceleration in units of SPEED / Velocity loop execution or SPEED / (SpdLpRate / PWM period). |

VelocityControl Write Register Field Definitions

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FaultControl Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|---|---|---|---|---|--------|---------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x42 | SPARE | | | | | | FltClr | DcBusM Enb |

FaultControl Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| DcBusMEnb | W | DC Bus monitor enable. 1 = Monitor DC bus voltage and generate appropriate brake signal control and disable PWM output when voltage fault conditions occur. GatekillFlt and OvrSpdFlt faults cannot be disabled. DC bus voltage thresholds are as follows: Overvoltage – 410V Brake On – 380V Brake Off – 360V Nominal – 310V Undervoltage off – 140V Undervoltage – 120V |
| FltClr | W | This bit clears all active fault conditions. The user should monitor the FaultStatus read register group to determine fault status and set this bit to “1” to clear any faults that have occurred. A fault condition automatically clears the PwmEnbW and FocEnbW bits in the SystemControl write register group. Note that this bit also directly controls the output 2137 FLTCLR pin. After clearing a fault, the user must explicitly set this bit to “0” to re-enable fault processing. |

FaultControl Write Register Field Definitions

SVPWMScaler Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|----------------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x44 | ModScl (LSBs) (W) | | | | | | | |
| 0x45 | ModScl (MSBs) (W) | | | | | | | |

SVPWMScaler Write Register Map

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| ModScl | W | Space vector modulator scale factor. This register, which depends on the PWM carrier frequency, should be set as follows: $\text{ModScl} = \text{PwmPeriod} * \text{sqrt}(3) * 4096 / 2355$ where PwmPeriod is the value in the PwmConfig write register group's PwmPeriod register. |

SVPWMScaler Write Register Field Definitions

DiagnosticPwmControl Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|---|---|---|-------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4E | PwmData1Sel | | | | PwmData0Sel | | | |
| 0x4F | PwmData3Sel | | | | PwmData2Sel | | | |

DiagnosticPwmControl Write Register Map

| Field Name | Access (R/W) | Field Description |
|---|--------------|---|
| PwmData0Sel, PwmData1Sel, PwmData2Sel, PwmData3Sel | W | Selects diagnostic data items for output on DAC PWM pins 0-3. These pins are intended for use with external RC filters for oscilloscope diagnostic display: 1 = DC Bus Voltage 2 = V phase current 3 = W phase current 5 = Speed PI Reference 6 = Speed PI Feedback 7 = Speed PI Error 8 = IQ Ref 9 = Q axis voltage Qv 10 = D axis voltage Dv 11 = 12-bit electrical angle 12 = Q axis current Qi 13 = D axis current Di 14 = A axis (stationary frame) voltage Av 15 = B axis (stationary frame) voltage Bv |

DiagnosticPwmControl Write Register Field Definitions

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SystemConfig Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|-----------|---|----------|---|-------------|------------|------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x50 | ExtCtrlW | SpdRefSel | | IqRefSel | | HostAng Enb | HostVd Enb | RmpRef Sel |

SystemConfig Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| RmpRefSel | W | Speed Ramp reference select. 0= TargetSpd field of the VelocityControl write register group, 1 = External analog reference. |
| HostVdEnb | W | Host D-Axis current control enable. When this bit is set, the D-Axis PI Controller is disconnected from the forward path vector rotator, which then takes its input from the VdSfwd field of the DirectHostVoltageControl write register group. |
| HostAngEnb | W | Host electrical angle control enable. When this bit is set, the vector rotator takes its angle input from the ElecAngW field of the DirectHostVoltageControl write register group. |
| IqRefSel | W | Selects the source for the Q-Axis PI controller IQREF input: 0 = Speed PI controller output 1 = IqRefW field of the CurrentLoopConfig write register group 2 = Reference A/D converter input. |
| SpdRefSel | W | Selects the source for the Speed PI controller reference input: 0 = Internal Accel/Deccel ramp generator 1 = TargetSpd field of the VelocityControl write register group 2 = Reference A/D converter input. |
| ExtCtrlW | W | Setting this bit to "1" enables direct control of basic motor operation via the external User Interface pins. When this bit is "1", the FocEnbW and PwmEnbW bits in the SystemControl write register group are ignored. |

SystemConfig Write Register Field Definitions

DirectHostVoltageControl Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|----------------------|---|---|---|----------------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x52 | VdSfwd (LSBs) (W) | | | | | | | |
| 0x53 | VqSfwd (LSBs) (W) | | | | VdSfwd (MSBs) (W) | | | |

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| Byte Offset | Bit Position | | | | | | | |
|-------------|------------------------|---|---|---|------------------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x54 | VqSfwd (MSBs) (W) | | | | | | | |
| 0x55 | ElecAngW (LSBs) (W) | | | | | | | |
| 0x56 | SPARE | | | | ElecAngW (MSBs) (W) | | | |

DirectHostVoltage Control Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|--|
| VdSfwd | W | 12-bit signed value for synchronous frame direct current when host direct current control is enabled. This field is typically used for V/Hz control. |
| VqSfwd | W | 12-bit signed value for synchronous frame quadrature voltage that is added to the Q-Axis PI-controller output. This field is typically used for feedforward or V/Hz control. |
| ElecAngW | W | 12-bit electrical angle used when host electrical angle control is enabled. This field is typically used for V/Hz control. |

DirectHostVoltageControl Write Register Field Definitions

32bitQuadDecode Register Group (Write Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------------------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x58 | EncCnt32bW (bits 0-7) (W) | | | | | | | |
| 0x59 | EncCnt32bW (bits 8-15) (W) | | | | | | | |
| 0x5A | EncCnt32bW (bits 16-23) (W) | | | | | | | |
| 0x5B | EncCnt32bW (bits 24-31) (W) | | | | | | | |

32bitQuadDecode Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|--|
| EncCnt32bW | W | New value for 32-bit Quadrature Decoder counter. |

32bitQuadDecode Write Register Field Definitions

EepromControl Registers (Write Registers)

At power up, the write registers can be optionally initialized with values stored in EEPROM. The EepromControl write register group and EepromStatus read register group are used to read and write these EEPROM values. Since the EeAddrW write register (which selects the EEPROM offset to read or write) does not require initialization at power up, the location corresponding to that register in EEPROM (at offset 0x5D) is used to store a register map version code. At power on, the IRMCK201 initializes the write registers from EEPROM only if the version code stored at this offset in EEPROM matches its internal register map version code (which can be read from the RegMapVer field of the EepromStatus read register group).

To enable write register initialization at power up, write the appropriate register map version code to EEPROM at offset 0x5D. To disable write register initialization at power up, write a zero (or any non-matching version code) to offset 0x5D of the EEPROM.

| Byte Offset | Bit Position | | | | | | | | |
|-------------|---------------------------------|---|---|---|---|---------|--------|-------|--|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x5C | SPARE | | | | | EeWrite | EeRead | EeRst | |
| 0x5D | EeAddrW / RegMapVersCode (W) | | | | | | | | |
| 0x5E | EeDataW (W) | | | | | | | | |

EepromControl Write Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| EeRst | W | Self-clearing EEPROM reset. Writing a "1" to this bit resets the I2C EEPROM interface. |
| EeRead | W | Self-clearing I2c EEPROM Read. Writing a "1" to this bit initiates an EEPROM read from the byte located at EEPROM address EeAddrW. After setting this bit the user should poll the EeBusy bit in the EepromStatus read register group to determine when the read completes and then read the data from EeDataR in the EepromStatus read register group. |
| EeWrite | W | Self-clearing EEPROM Write. Writing a "1" to this bit initiates an EEPROM write from the data byte in EeDataW to the EEPROM address EeAddrW. |
| EeAddrW | W | EEPROM Address Register. Contains the address for the next EEPROM read or write operation. |
| EeDataW | W | EEPROM Data Register. Contains the data for the next EEPROM write operation. |

EepromControl Write Register Field Definitions

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HallSensorEncoderInit (Write Registers – EEPROM only)

These values must be set in the EEPROM for initial encoder count/angle initialization in the EEPROM standalone (i.e. operation without a host program). EEPROM initialization logic automatically loads the appropriate value into the encoder counter at power-on based on the HALL A/B/C sensor values. These values are present only in the EEPROM since they serve no purpose after power on.

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x72 | HallCBA001(LSBs) | | | | | | | |
| 0x73 | HallCBA001(MSBs) | | | | | | | |
| 0x74 | HallCBA010 (LSBs) | | | | | | | |
| 0x75 | HallCBA010 (MSBs) | | | | | | | |
| 0x76 | HallCBA011(LSBs) | | | | | | | |
| 0x77 | HallCBA011(MSBs) | | | | | | | |
| 0x78 | HallCBA100 (LSBs) | | | | | | | |
| 0x79 | HallCBA100 (MSBs) | | | | | | | |
| 0x7A | HallCBA101(LSBs) | | | | | | | |
| 0x7B | HallCBA101(MSBs) | | | | | | | |
| 0x7C | HallCBA110 (LSBs) | | | | | | | |
| 0x7D | HallCBA 110 (MSBs) | | | | | | | |

HallSensorEncoderInit Register Map

| Field Name | Access (R/W) | Field Description |
|---------------|--------------------|--|
| HallCBA nnn | W (EEPROM ONLY) | Initial encoder count for Hall Sensor [C, B, A] value [n , n , n]. |

HallSensorEncoderInit Field Definitions

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Read Register Definitions

QuadratureDecodeStatus Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|-----------------------|----------------|----------------|----------------|-------|-------|-------|-------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 | EncCntR (LSBs) (R) | | | | | | | |
| 0x1 | EncCntR (MSBs) (R) | | | | | | | |
| 0x3 | SPARE | PwrOn HallC | PwrOn HallB | PwrOn HallA | SPARE | HallC | HallB | HallA |

QuadratureDecodeStatus Read Register Map

| Field Name | Access (R/W) | Field Description |
|------------------------------------|--------------|--|
| EncCntR | R | Current value of 16-bit Quadrature Decoder counter. |
| HallA, HallB, HallC | R | Hall Sensor A/B/C values. |
| PwrOnHallA, PwrOnHallB, PwrOnHallC | R | Hall Sensor A/B/C values at power-on for reduced-wire encoder interface. |

QuadratureDecodeStatus Read Register Field Definitions

SystemStatus Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|----------------|------|-------|-------|---|----------|-------------|-------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x7 | Start | Stop | SPARE | PwrID | | GateKill | Foc EnbR | Pwm EnbR |
| 0x8 | RevCode (LSBs) | | | | | | | |
| 0x9 | RevCode (MSBs) | | | | | | | |

SystemStatus Read Register Map

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| PwmEnbR | R | PWM Enable bit status. |
| FocEnbR | R | FOC Enable bit status. |
| GateKill | R | GATEKILL status. This bit is set by the Gatekill input from the IR2137. Once set, this bit remains set until it is cleared by writing a "1" to the FaultClr bit in the FaultControl write register group. |
| PwrID | R | Power ID. 0 = 3 kW, 1 = 2 kW, 2 = 500 W. |
| Stop | R | User Interface "STOP" digital input status. |
| Start | R | User Interface "START" digital input status. |
| RevCode | R | IC Revision Code. Revision code format is "XX.XX", where each "X" is a 4-bit hexadecimal number. |

SystemStatus Read Register Field Definitions

DcBusVoltage Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|-------------------|---|---|-------|---|-------------------|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xA | DcBusVolts (LSBs) | | | | | | | |
| 0xB | SPARE | | | Brake | | DcBusVolts (MSBs) | | |

DcBusVoltage Read Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|--|
| DcBusVolts | R | DC Bus Voltage. Data range is 0 - 4095, which corresponds to a DC bus voltage between 0 and 500 volts. |
| Brake | R | Brake signal status. 0 = Brake signal active. |

DcBusVoltage Read Register Field Definitions

FocDiagnosticData Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xC | IvFbk - V Phase IFB Raw Current (LSBs) (R) | | | | | | | |
| 0xD | IwFbk - W Phase IFB Raw Current (LSBs) (R) | | | | IvFbk - V Phase IFB Raw Current (MSBs) (R) | | | |

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| Byte Offset | Bit Position | | | | | | | |
|-------------|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0xE | IwFbk - W Phase IFB Raw Current (MSBs) (R) | | | | | | | |
| 0xF | Id – Synchronous Frame Direct Current (LSBs) (R) | | | | | | | |
| 0x10 | Id – Synchronous Frame Direct Current (MSBs) (R) | | | | | | | |
| 0x11 | Iq – Synchronous Frame Quadrature Current (LSBs) (R) | | | | | | | |
| 0x12 | Iq – Synchronous Frame Quadrature Current (MSBs) (R) | | | | | | | |
| 0x13 | Ud – Synchronous Frame Direct Voltage (LSBs) (R) | | | | | | | |
| 0x14 | Ud – Synchronous Frame Direct Voltage (MSBs) (R) | | | | | | | |
| 0x15 | Uq – Synchronous Frame Quadrature Voltage (LSBs) (R) | | | | | | | |
| 0x16 | Uq – Synchronous Frame Quadrature Voltage (MSBs) (R) | | | | | | | |
| 0x17 | UAlpha – Stationary Frame Alpha Voltage (LSBs) (R) | | | | | | | |
| 0x18 | UBeta – Stationary Frame Beta Voltage (LSBs) (R) | | | | UAlpha – Stationary Frame Alpha Voltage (MSBs) (R) | | | |
| 0x19 | UBeta – Stationary Frame Beta Voltage (MSBs) (R) | | | | | | | |

FocDiagnosticData Read Register Map

| Field Name | Access (R/W) | Field Description |
|--------------|--------------|---|
| IvFbk, IwFbk | R | Offset-corrected V and W phase raw current from the IR2175 current sensor. Values range from 0 - 4096, where 2048 corresponds to 0 current. The current feedback scale factors IdScl and IqScl in the CurrentFeedbackConfig write register group and the current sense resistor value determine the full scale current value. |
| Id, Iq | R | Synchronous or rotating frame direct and quadrature current values in 2's complement representation. The full scale current values range from -16384 to 16383. |
| Ud, Uq | R | Synchronous or rotating frame direct and quadrature voltage values in 2's complement representation. Data ranges are $\pm VdLim$ for Ud and $\pm VqLim$ for Uq as specified in the CurrentLoopConfig write register group. |

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| | | |
|------------------|---|--|
| UAlpha, UBeta | R | Stationary frame Alpha and Beta voltage output component values. Data range is $\pm VdLim$ or $\pm VqLim$ (as specified in the CurrentLoopConfig write register group), whichever is larger. |
|------------------|---|--|

FocDiagnosticData Read Register Field Definitions

FaultStatus Register Group (Read Registers)

The Fault Status register records fault conditions that occur during drive operation. When any of these fault conditions occur, the PWM output is automatically disabled. The user should monitor this register continuously for fault conditions. A fault condition can be cleared by writing a “1” to the FaultClr bit in the FaultControl write register group. (This does not automatically re-enable PWM output.)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|---|---|------------|-----------|-------|-------|-------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x1E | SPARE | | | ExecTm Flt | OvrSpdFlt | OvFlt | LvFlt | GatekillFlt |

FaultStatus Read Register Map

| Field Name | Access (R/W) | Field Description |
|-------------|--------------|---|
| GatekillFlt | R | Filtered and latched version of IR213x FAULT output. |
| LvFlt | R | DC bus low voltage fault. This fault occurs if the DC bus drops below 120V. |
| OvFlt | R | DC bus overvoltage fault. This fault occurs if the DC bus voltage exceeds 410V. |
| OvrSpdFlt | R | Over speed fault. This fault occurs whenever the motor reaches the positive or negative limits. The user should use the scale factor in the SpdScl field of the VelocityControl write register group to scale the motor speed so that it falls between -16384 and +16383 with these limits as the over speed condition. |
| ExecTmFlt | R | Execution time fault. |

FaultStatus Read Register Field Definitions

VelocityStatus Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x26 | Spd (LSBs) | | | | | | | |
| 0x27 | Spd (MSBs) | | | | | | | |

VelocityStatus Read Register Map

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|--|
| Spd | R | Current motor speed in SPEED units. (See the description of SpdScl in the VelocityControl write register group.) |

VelocityStatus Read Register Field Definitions

CurrentFeedbackOffset Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|------------------------|---|---|---|------------------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x30 | IfbVOffs (LSBs) (R) | | | | | | | |
| 0x31 | IfbWOffs (LSBs) (R) | | | | IfbVOffs (MSBs) (R) | | | |
| 0x32 | IfbWOffs (MSBs) (R) | | | | | | | |

CurrentFeedbackOffset Read Register Map

| Field Name | Access (R/W) | Field Description |
|--------------------|--------------|--|
| IfbVOffs, IfbWOffs | R | Current feedback offset values from the last IFB Offset calculation. These values are automatically applied to each current feedback measurement value whenever the IfbOffsEnb bit in the SystemControl write register group is set. |

CurrentFeedbackOffset Read Register Field Definitions

32bitQuadDecodeStatus Register Group (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|--------------------------------|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x34 | EncCnt32bR (bits 0-7) (R) | | | | | | | |
| 0x35 | EncCnt32bR (bits 8-15) (R) | | | | | | | |
| 0x36 | EncCnt32bR (bits 16-23) (R) | | | | | | | |
| 0x37 | EncCnt32bR (bits 24-31) (R) | | | | | | | |

32bitQuadDecodeStatus Read Register Map

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| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| EncCnt32bR | R | Current value of 32-bit Quadrature Decoder counter. |

32bitQuadDecodeStatus Read Register Field Definitions

EepromStatus Registers (Read Registers)

| Byte Offset | Bit Position | | | | | | | |
|-------------|---------------|---|---|---|---|---|---|--------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x38 | SPARE | | | | | | | EeBusy |
| 0x39 | EeDataR (R) | | | | | | | |
| 0x3A | EeAddrR (R) | | | | | | | |
| 0x3B | RegMapVer (R) | | | | | | | |

EepromStatus Read Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|---|
| EeBusy | R | I2C EEPROM Interface busy bit. The user should wait for this bit to clear before initiating EEPROM read or write operations. |
| EeDataR | R | EEPROM Data Register. Contains the data from the last EEPROM read operation. Note that writing to the EeRst field in the EepromControl write register group invalidates this register. |
| EeAddrR | R | EEPROM Address read register shows the value stored in EEPROM at the offset of the EeAddrW write register (0x5D). Since this address in the EEPROM contains the IRMCK201 register map version, the user can read this field to determine whether or not the write registers were initialized at power on. |
| RegMapVer | R | Current register map version code. |

EepromStatus Read Register Field Definitions

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FOCDiagnosticDataSupplement Register Group (Read Registers)

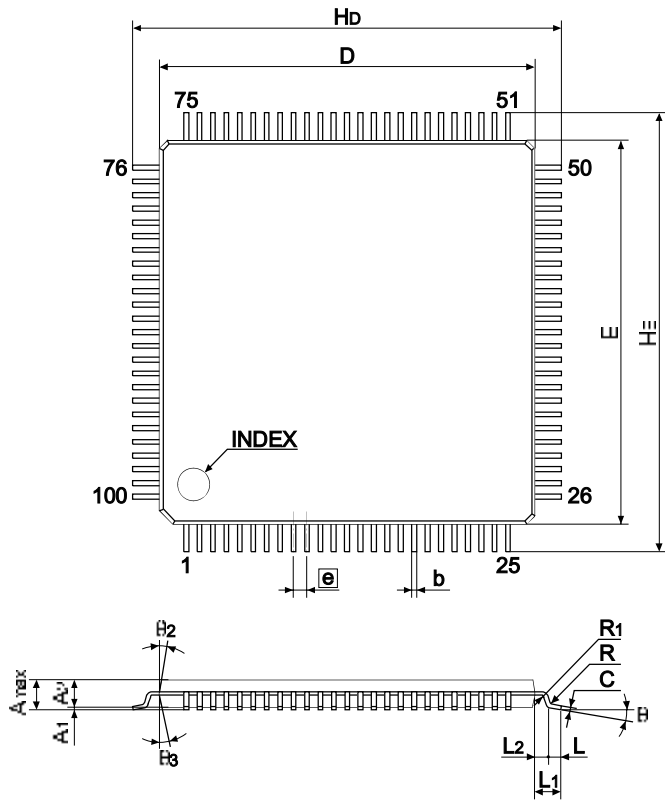
| Byte Offset | Bit Position | | | | | | | |
|-------------|------------------------|---|---|---|------------------------|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x3C | ElecAngR (LSBs) (R) | | | | | | | |
| 0x3D | SPARE | | | | ElecAngR (MSBs) (R) | | | |
| 0x3E | SpdRef (LSBs) (R) | | | | | | | |
| 0x3F | SpdRef (MSBs) (R) | | | | | | | |
| 0x40 | SpdErr (LSBs) (R) | | | | | | | |
| 0x41 | SpdErr (MSBs) (R) | | | | | | | |
| 0x42 | IqRefR (LSBs) (R) | | | | | | | |
| 0x43 | IqRefR (MSBs) (R) | | | | | | | |

FOCDiagnosticDataSupplement Read Register Map

| Field Name | Access (R/W) | Field Description |
|------------|--------------|--------------------------------------|
| ElecAngR | R | Electrical angle. |
| SpdRef | R | Speed PI controller reference input. |
| SpdErr | R | Speed PI controller error. |
| IqRefR | R | Speed PI controller output. |

FOCDiagnosticDataSupplement Read Register Field Definitions

Plastic QFP 100pin Body size 14 x 14 x 1.4mm (QFP15)



Lead type STD (QFP15-100pin STD)

| Symbol | Dimension in Millimeters | | | Dimension in Inches * | | |
|--------|--------------------------|-------|-------|-----------------------|---------|---------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| E | 13.9 | 14 | 14.1 | (0.548) | (0.551) | (0.555) |
| D | 13.9 | 14 | 14.1 | (0.548) | (0.551) | (0.555) |
| A | | | 1.7 | | | (0.066) |
| A1 | | 0.1 | | | (0.004) | |
| A2 | 1.3 | 1.4 | 1.5 | (0.052) | (0.055) | (0.059) |
| e | | 0.5 | | | (0.020) | |
| b | 0.13 | 0.18 | 0.28 | (0.006) | (0.007) | (0.011) |
| C | 0.1 | 0.125 | 0.175 | (0.004) | (0.005) | (0.006) |
| H | 0° | | 10° | (0°) | | (10°) |
| L | 0.3 | 0.5 | 0.7 | (0.012) | (0.020) | (0.027) |
| L1 | | 1 | | | (0.039) | |
| L2 | | 0.5 | | | (0.020) | |
| HE | 15.6 | 16 | 16.4 | (0.615) | (0.630) | (0.645) |
| Hd | 15.6 | 16 | 16.4 | (0.615) | (0.630) | (0.645) |
| H2 | | 12° | | | (12°) | |
| R3 | | 12° | | | (12°) | |
| R | | 0.2 | | | (0.008) | |
| R1 | | 0.2 | | | (0.008) | |

* for reference

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| SYMBOL | DIMENSION IN MILLIMETERS | | | DIMENSION IN INCHES* | | |
|----------------|--------------------------|-------|-------|----------------------|---------|---------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| E | 13.9 | 14 | 14.1 | (0.548) | (0.551) | (0.555) |
| D | 13.9 | 14 | 14.1 | (0.548) | (0.551) | (0.555) |
| A | | | 1.7 | | | (0.066) |
| A1 | | 0.1 | | | (0.004) | |
| A2 | 1.3 | 1.4 | 1.5 | (0.052) | (0.055) | (0.059) |
| e | | 0.5 | | | (0.020) | |
| b | 0.13 | 0.18 | 0.28 | (0.006) | (0.007) | (0.011) |
| C | 0.1 | 0.125 | 0.175 | (0.004) | (0.005) | (0.006) |
| θ | 0° | | 10° | (0°) | | (10°) |
| L | 0.3 | 0.5 | 0.7 | (0.012) | (0.20) | (0.027) |
| L1 | | 1 | | | (0.039) | |
| L2 | | 0.5 | | | (0.020) | |
| H _E | 15.6 | 16 | 16.4 | (0.615) | (0.630) | (0.645) |
| H _D | 15.6 | 16 | 16.4 | (0.615) | (0.630) | (0.645) |
| O2 | | 12° | | | (12°) | |
| O3 | | 12° | | | (12°) | |
| R | | 0.2 | | | (0.008) | |
| R1 | | 0.2 | | | (0.008) | |

Table 27: QFP100 Dimensions

*** For reference**

Appendix C Errata

1. Using the ADS7818 A/D converter interface as the current feedback source is not supported
2. The scaling is too large by a factor of 16 for the following Diagnostic DAC PWM selections: Reference Speed (PWM data select value of 5), Motor Speed (PWM data select value of 6), IQREF (PWM data select value of 8).

The scaling is too large by a factor of 8 for the following Diagnostic DAC PWM selections: IQ (PWM data select value of 12), ID (PWM data select value of 13).

The scaling is too large by a factor of 4 for the following Diagnostic DAC PWM selections: Av (PWM data select value of 14), Bv (PWM data select value of 15).

These values will work at small data ranges, but overflow otherwise. To extract the correct data for these items, use the parallel port and diagnostic data registers.
3. When the IRMCK201 is implemented in conjunction with the ADS7818, note that the IRMCK201 ADCLK is specified at 120 ns while the ADS7818 is specified at 125 ns.

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